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Compact Digitizing and Serializing for the ATLAS Level-1 Calorimeter Trigger

Diploma Thesis in Physics

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under the supervision of

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Compact Digitizing and Serializing
for the ATLAS Level-1 Calorimeter Trigger

This thesis describes the developments towards a Multi-Chip Module for the ATLAS Level-1 Calorimeter Trigger. This Multi-Chip Module does most of the preprocessing tasks. Some of these include the digitization of analog trigger tower signals from the ATLAS Calorimetry and the high-speed serial data transmission to the subsequent trigger processors. Six demonstrator MCMs have been assembled for the Pre-Processor Modular Test System. For the final Pre-Processor Multi-Chip Module, changes were made in the digitization precision from 8-bits to 10-bits, and the G-link serializers were changed to LVDS serializers. To investigate the interplay of these new components and to evaluate layout properties, an intermediate step between the demonstrator MCM and the final Pre-Processor MCM has been inserted in the form of a CMC card, called the ECMC. The ECMC card has been successfully designed, manufactured and brought into operation. Several tests have been performed with the aim to evaluate layout properties for the final PPrMCM and to investigate the interplay of the used chips and the performance of the digitization.

Kompaktes Digitalisieren und Serialisieren
für den ATLAS Level-1 Kalorimeter Trigger

Diese Arbeit beschreibt Entwicklungen für ein Multi-Chip Module (MCM), das die meisten Vorverarbeitungsaufgaben für den ATLAS Level-1 Kalorimeter Trigger ausführt. Diese beinhalten das Digitalisieren von analogen Triggerzellensignalen vom ATLAS Kalorimeter und die serielle Datenübertragung zu den nachfolgenden Triggerprozessoren. Sechs MCM Prototypen wurden für das Modulare Test System des Pre-Prozessors bestückt. Für das finale Pre-Prozessor Multi-Chip Module wurden Änderungen in der Digitalisierungsgenauigkeit von 8-bits auf 10-bits vorgenommen und von G-link Serialisierern zu LVDS Serialisierern gewechselt. Um das Zusammenspiel dieser neuen Komponenten zu untersuchen und um Layouteigenschaften auszuwerten, wurde ein Entwicklungsschritt zwischen dem MCM Prototypen und dem finalen Pre-Prozessor MCM in Form einer CMC Karte mit dem Namen ECMC eingefügt. Diese ECMC Karte wurde erfolgreich entworfen, hergestellt und in Betrieb genommen. Mehrere Tests wurden durchgeführt, die zum Ziel hatten, Layouteigenschaften des finalen PPrMCM zu bestimmen, das Zusammenspiel der benuzten Chips und die Leistungsfähigkeit der Digitalisierung zu untersuchen.

Contents

Introduction

Science will always have borders,
but no eternal borders.

P. du Bois-Reymond

Within living memory, people have always struggled to understand the world around them. With the concept of experimental physics and the development of mathematical theories which describe the experimental results, an enormous progress in knowledge about the world and its basic constituents has been obtained.

The discovery of relativity and quantum mechanics has been revolutionary for the perception of the world. From the atom to the nuclei to neutrons and protons to quarks, the use of particle accelerators have taken off layer after layer of the structure of matter. The necessity for experiments at high energies has led to the construction of large and complex particle accelerators in order to penetrate deeper into the substance of matter. The next generation of high-energy physics has to operate in the TeV range in order to address new and open issues of particle physics.

The increase in size, complexity and costs of the detectors for high energy physics experiments has led to world-wide collaborations of physics institutes and research centers, all combining their efforts in a common goal. The ATLAS experiment at the Large Hadron Collider will be the largest detector built in history and the biggest joint venture in the physical science. The ATLAS detector will have the potential to detect yet undiscovered particles like the Higgs boson and supersymmetric particles and to resolve smallest structures.

The amount of data produced in such high energy collissions is enormous. Data from particle detection, energy measurements, track reconstruction etc. for millions of particles is generated. The data volume is so huge that it cannot be recorded. Therefore, a sophisticated trigger has to distinguish between interesting and non-interesting events in order to reduce the data quantity to a storeable size.

This thesis deals with some aspects of the design of the Level-1 Trigger, the first level of event selection. A Multi-Chip Module does most of the pre-processing tasks for the ATLAS Level-1 Calorimeter Trigger. This includes the digitization of analog trigger tower signals from the ATLAS Calorimetry, bunch-crossing identification (BCID), calibration of the transverse energy, read-out of raw trigger data and high-speed serial data transmission to the subsequent trigger processors.

Chapter 1

Physical Overview

1.1 The Standard Model

The experimental discoveries and theoretical developments of the last 50 years led to the development of the Standard Model (SM) of particle physics. Since it is subject of a lot of articles and particle physics books [1][2], this section will just give a brief summary.

The Standard Model is a gauge field theory with local gauge invariance and describes all of the known fundamental particles and their interactions, namely, the electromagnetic interaction, the weak interaction and the strong interaction. The gravitational interaction, which is by far the weakest out of the four fundamental interactions, is not described by the Standard Model. Table 1.1 gives an overview of the four fundamental interactions. The fundamental particles can be grouped in three different groups according to their spin.

Interaction	**Gauge Bosons**	**Acts on**	**Strength**
electromagnetic	photon (γ)	electric charge	$\alpha = 1/137$
weak	$W^{\pm}, Z^0$	flavor	$\alpha_{weak} = 0.03$
strong	gluons (g)	color charge	$\alpha_s \approx 0.12..1$
gravity	graviton (G)	mass	-

Table 1.1: Fundamental interactions and gauge bosons.

Fermions carry a spin of 1/2, bosons have spin 1 and the Higgs boson has spin 0. Normal matter is made of fermions. The up and down quarks, the electron and the electron neutrino are the constituents that ourselves and the world are made of. For unknown reasons, this pattern of basic building blocks of two quarks, a lepton and a neutrino is repeated three times making three generations of fermions. Table 1.2 gives a summary of all fermions with their corresponding masses and electric charges.

The strong, the weak and the electromagnetic interaction are all very similar in their structure and can be explained by exchanging intermediate vector bosons. The electromagnetic interaction is described by quantum electrodynamics (QED), a gauge field theory which describes the interaction between charged particles via exchange of a spin 1 gauge boson, the photon. It is an extremely successful theory as their predictions match very

Quarks			Leptons		
Flavor	Charge	Mass [MeV]	Flavor	Charge	Mass [MeV]
u	$+2/3$	1.5..5	ν_{e}	0	$< 1.5 \times 10^{-6}$
d	$-1/3$	3..9	e^-	-1	0.511
c	$+2/3$	1100..1400	ν_μ	0	$< 1.9 \times 10^{-4}$
s	$-1/3$	60..170	μ^-	-1	105.7
t	$+2/3$	$170..179 \times 10^3$	ν_τ	0	< 18.2
b	$-1/3$	4100..4400	τ^-	-1	< 1777.1

Table 1.2: Fundamental fermions of the Standard Model

precisely with experimentally observed properties.

The strong interaction can also be described by a gauge field theory, called quantum chromodynamics, which has been developed according to QED. There we have eight gauge bosons, called gluons, which mediate the interaction of particles carrying color. A quark can occur in 3 different colors and a gluon always carries one color and one anti-color. The fact that the gauge boson themselves are colored objects makes it possible for them to interact between eachother. Another characteristic of the strong interaction is that at high energy scales, and therefore small distances, the strong interaction becomes weaker, or 'asymptotically free'. At lower energies and accordingly longer scales, the interaction between the particles becomes stronger. This behaviour may explain why colored objects have not yet been observed isolated, only 'confined' in colorless objects.

The weak and the electromagnetic interaction are described in the unified theory of the electroweak interaction of Glashow, Salam and Weinberg. In this theory the weak interaction is mediated by three massive vector bosons, the Z^0, W^+ and W^-, which were found experimentally in 1984 at CERN [3][4].

Allowing massive gauge bosons while maintaining the necessary renormalisability for the gauge theory requires the so-called Higgs mechanism. Massless gauge bosons result in an infinite reach of the mediated interaction and therefore to an '1/r form' of the corresponding potential. In the case of massive gauge bosons with mass m, the corresponding potential is shielded by a term e^{-mr}. This is also the reason why the weak interaction is not relevant for macroscopic systems and therefore has been called 'weak'. However, at distances which are in the order of $\frac{1}{m}$, the weak interaction has comparable strength to the electromagnetic interaction. The weakness results from the mass of the gauge bosons.

If one defines mass as the attribute, that a particle with given energy E travels slower than with the 'natural' velocity c then there must be something that hinders the particle to travel with the speed of light. This interference can be described by a permanent interaction of the particle with a field which does not disappear in the quantum mechanical vacuum. In the Standard Model, this field, the Higgs-field is a complex doublet with four real components. The idea behind the theory is, that all particles are interacting with this field, and therefore behave as though they were to have an effective mass. The value of the mass depends on the strength of the coupling to the Higgs-field. Three degrees of freedom of the postulated Higgs-field are used to describe the three longitudinal degrees of freedom for the spins of the three massive gauge bosons Z^0, W^+ and W^-. The forth degree of freedom corresponds to an excited state of the Higgs-field, which should, if this field exists, be observable as a massive scalar particle, the Higgs-particle. The Higgs-particle has not been observed yet, and is the last missing particle of the Standard Model.

1.1.1 Troubles of the Standard Model

Even though experimental results show a stunning agreement with the predictions of the Standard Model, there are still a number of unanswered questions:

- There are 18 free parameters, which must be put in 'by hand', like the masses of fermions and bosons or the coupling constants of the interactions.
- Why are there three generations of fermions?
- What is the origin of electroweak symmetry breaking?
- What is the origin of P and CP violation?
- Why is there more matter than anti-matter?
- What is dark matter made of?

1.1.2 Beyond the Standard Model

Unification

To obtain a final theory, theoretisists attempt to find a theory which unifies the strong with the electroweak interaction. In such a theory, all particle interactions can be described and only one coupling constant g_G is necessary. The two coupling constants of the electroweak interaction g and g', and g_s of the strong interaction, would then be related to g_G. As the coupling strength is a function of the momentum transfer Q, all three interactions should have the same coupling strength at some large energy M_x. As predicted by electroweak

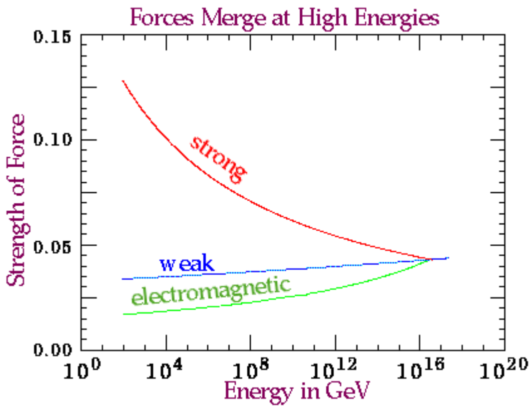


Figure 1.1: The strength of the three forces merge at high energy [5].

theory and quantum chromodynamics, M_x is expected to be around 10^{16} GeV. Figure 1.1 shows the variation of the coupling constants with Q. These Grand Unified Theories (GUT) share some of the problems of the Standard Model. For example, too many arbitrary parameters and no interaction with gravity.

Supersymmetry

All supersymmetric extensions to the Standard Model propose a symmetry between fundamental fermions and bosons. Leptons and quarks have sleptons and squarks, which are bosons, as supersymmetric partners. The partner of the gauge bosons and the Higgs bosons are gaugino fermions and the fermionic sHiggs particle. At some stage, the symmetry between bosons and fermions proposed by supersymmetric theories must have been broken to explain why SUSY particles have not yet been observed.

In most SUSY theories, sparticles have to be produced in pairs, leading to a quantum number R, which must be conserved. Particles have an R value of $+1$ and sparticles -1. The conservation of R implies that at least the lightest sparticle must be stable, as there is no supersymmetric particle into which it can decay. In the Minimal Supersymmetric Standard Model (MSSM), SUSY requires at least two complex Higgs doublets (H_1, H_2). It thus has at least five physical neutral and charged Higgs bosons, where the lightest is to be expected to have a mass of about 130 GeV. To date, there has been no evidence for the existence of supersymmetric particles.

1.2 Proton-Proton Physics

As protons are no elementary particles, they consist of partons, the quarks and the gluons. An individual proton is made of three valence quarks and a sea of virtual quarks and gluons. The interaction between these partons is described, as previously mentioned, by QCD. In order to calculate predictions in QCD, and all other gauge theories, one uses the method of pertubation theory. Unfortunately pertubation theory is only valid when the coupling constant α is small compared to one. As the coupling constant of the strong interaction α_s becomes rather big at small energies and therefore large distances (confinement), pertubation theory cannot be used for QCD describing parton interactions at low energies. In such cases one has to use phenomenological models, like string theory. This makes calculations in QCD much more complicated.

The scattering process

The total momentum of the proton P is shared by all partons within the proton. The probability that a parton carries the portion x of the proton momentum is given by the structure function $F_2(x, Q^2)$, which is obtained by experimental measurements. During the elastic scattering of two protons, the structure of the colliding protons remain stable and are only slightly deflected. At inelastic scatterings with high momentum transfer however, only two partons of the proton with the portion of momentum x_1 and x_2, participate in the collision process. The partons which are not involved in the inelastic scattering proceed further almost untouched and form jets with high longitudinal momentum through hadronization. Figure 1.2 shows a schematic view of this inelastic scattering process. Another possibility of interaction between two partons is the fusion or the annihilation of

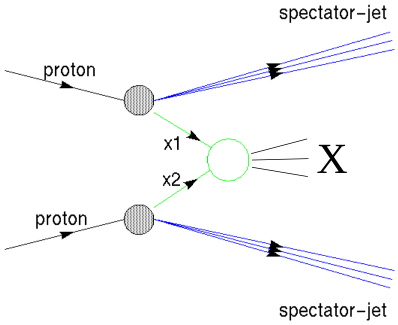


Figure 1.2: The scattering process in the parton model.

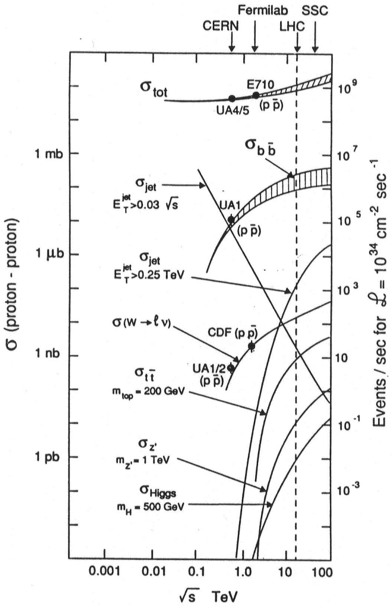


Figure 1.3: Cross-section of proton-proton interactions [6].

partons. The available center of mass energy $\sqrt{s}$ of an annihilated parton pair results to $\sqrt{x_1 x_2 s}$ reduced by the factors x_1 and x_2 compared to the original center of mass energy of the two protons. Most of the processes which are observed at proton-proton collisions are simple processes with very low momentum transfer. They contribute the main part to the total cross-section of proton-proton scattering. Interesting processes, like the production of heavy quarks and jets with high transverse momentum are rare. This is also the case for theoretically predicted particles like the Higgs boson and SUSY particles. Figure 1.3 shows the total cross-section of proton-proton collisions and the cross-section for heavy quark and Higgs boson production as a function of the center of mass energy $\sqrt{s}$. It can be seen, that for example the cross-section for Higgs-boson production is tiny compared to the total cross-section ($\sigma_{Higgs}/\sigma_{tot} \approx 10^{-11}$).

Chapter 2

The ATLAS Experiment at the LHC

2.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is a proton-proton collider being built at CERN in Geneva, due to be ready for operation in 2005. At that time, it will be the world's highest energy collider, accelerating two counter-rotating beams with a center of mass energy of 14 TeV and a peak luminosity[1] of $10^{34}cm^{-2}s^{-1}$. The LHC will be installed in the 27 km circumference LEP tunnel. The accelerator chain consists of a 50 MeV linac, the 1.4 GeV PS booster, the 26 GeV PS and the 450 GeV SPS. The accelerator chain and the LHC ring are shown in Figure 2.1.

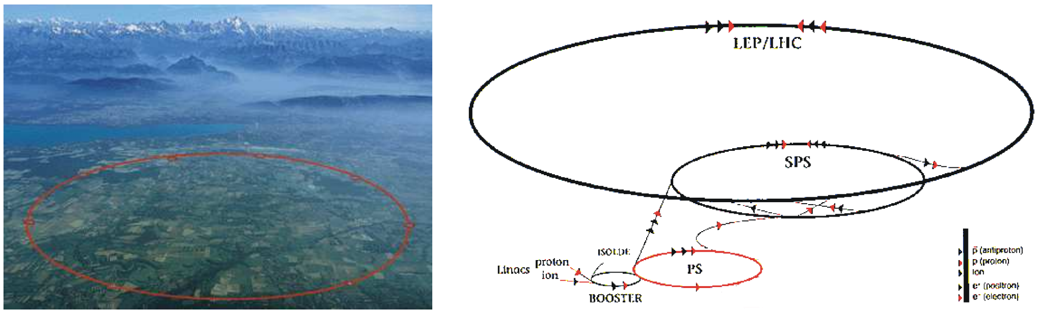


Figure 2.1: The LHC from a bird's eye view and the LHC accelerator chain [7].

The LHC will also be used as a heavy ion (Pb-Pb) collider, reaching a center of mass energy of up to 1250 TeV and a peak luminosity of $10^{27}cm^{-2}s^{-1}$. Since the LHC will collide beams with the same charge, two separate beam lines are necessary to allow the two beams to circulate in opposite directions and collide on the interaction points, where the beam lines are crossed. Due to space restrictions in the LEP tunnel being used, a magnet design

[1] Luminosity is the number of particles crossing a unit area per unit time. It can be calculated by $L = \frac{fN_1N_2}{A}$ where N_1 and N_2 are the number of particles in each bunch, A the cross-sectional area of the beam and f the frequency.

was chosen that combines the two guiding fields into a single dipole magnet as shown in Figure 2.2.

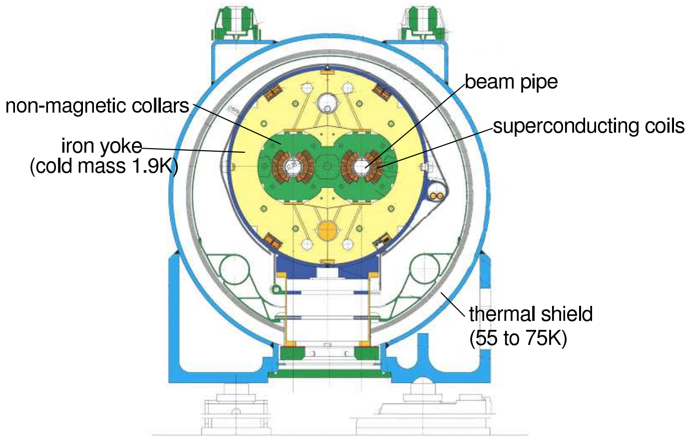


Figure 2.2: The cross-section of an LHC two-in-one dipole [8].

In order to meet the stringent requirements in luminosity and energy, the dipole magnets must be superconductive, cooled by superfluid helium with a field strength of about 8.33 Tesla. In total, 1296 dipole magnets will be necessary. For beam focusing, 6.9 Tesla superconductive quadrupole magnets are used in combination with several other elements providing fine tuning.

In the beamline, the protons are stored in bunches, where each bunch contains about 10^{11} protons. Along the ring a total number of 2961 bunches are stored, separated with a bunch spacing of 25 ns. Table 2.1 summarizes the LHC performance parameters. The ring

LHC performance parameters	
Center of mass energy	14 TeV
Circumference	27 km
Dipole field	8.33 T
Luminosity	$10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Injection energy	450 GeV
Bunch separation	25 ns
Bunch spacing	7.5 m
Particles per bunch	10^{11}
Stored beam energy	334 MJ
Beam lifetime	22 h
Luminosity lifetime	10 h
Energy loss per turn	6.7 keV

Table 2.1: LHC performance parameters

layout has eight long straight sections, each about 500 m long, where experimental utilities can be inserted. Always at two straight sections, the beamlines from the counter-rotating beams cross, giving four experiments the possibility to detect collision fragments. Figure 2.3 shows the location of the four experiments being planned for the LHC.

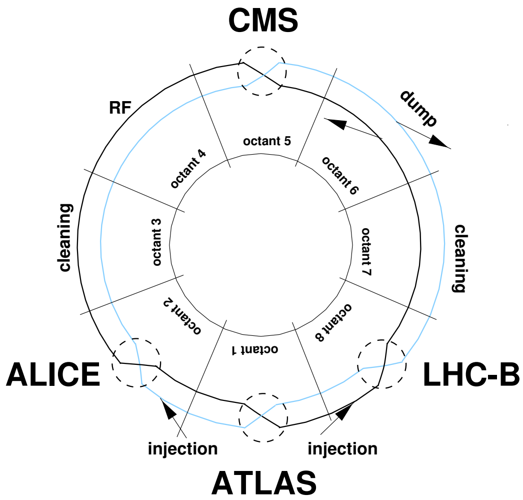


Figure 2.3: The location of the four planned experiments at the LHC [9].

ALICE (**A** **L**arge **I**on **C**ollider **E**xperiment) in octant 2 will be dedicated to heavy ion collisions at very high energies. The aim is to study strongly interacting matter at extreme energy densities.

LHC-b(**LHC** **b**ottom-quarks) located in octant 8 will be a single-arm spectrometer focusing onto the forward direction of the interaction point. This provides very good possibilities to study CP violation in the B sector.

In octant 1 and 5 located in opposite straight sections, two general purpose detectors **CMS** (**C**ompact **M**uon **S**olenoid) and **ATLAS** (**A** **T**oroidal **L**HC **A**paratus) will be installed. The latter will be the focus of the following sections.

2.2 Physics at ATLAS

The LHC offers an unprecedented range of opportunity for physics studies. The physical program can be roughly summarized to precision measurements of the Standard Model, the search for the Higgs boson and search for physics beyond the Standard Model.

The major focus of interest for ATLAS is the Higgs particle. ATLAS is designed to cover a wide mass range for a potential detection of the Higgs particle from about 80 GeV up to 1 TeV. However, since ATLAS was planned the possible mass range for the Higgs particle has narrowed down. Figure 2.4 shows the result of an analysis of indirect electroweak precision measurements performed by the LEP Collaboration on combined data from ALEPH, DELPHI, L3 and OPAL. In this graph, the Higgs mass is plotted versus $\Delta\chi^2$, showing a minimum for the Higgs mass around 100 GeV. This result shows, that ATLAS has to search in the small mass range of it's large potential. Direct searches at LEP were able to exclude a Higgs boson with a mass below approximately 95 GeV, this corresponds to the grey area in the graph.

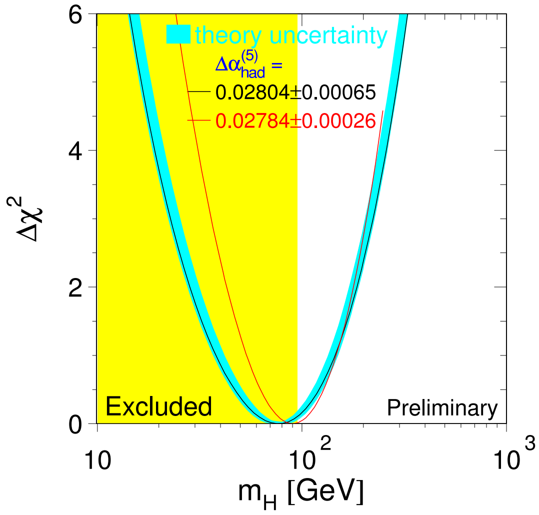


Figure 2.4: The most probable Higgs mass [10].

Another prominent goal for the LHC is the search for supersymmetry, a proof for physics beyond the Standard Model. If supersymmetry exists, a rich production of new particles is expected to occur at the LHC, giving ATLAS the possibility to make precise measurements of the properties of theses yet unseen particles.

The LHC will also allow to perform high precision measurements for the top quark and the W mass, due to a high production rate of eight million tt pairs and three hundred million single W per year.

In the QCD sector, the access to never reached energies can address open questions to the compositness of quarks and make precise measurements of the parton distribution functions.

The above physics program, described in greater detail in the ATLAS Detector and Physics Performance Technical Design Report [11], leads to the following basic requirements for the ATLAS detector:

- Very good electromagnetic calorimetry for electron and photon identification and measurements.
- Full coverage hadronic calorimetry for accurate jet and missing transverse energy measurements.
- High precision muon momentum measurements.
- An effective tracking system capable of high p_t lepton measurements, electron, photon, tau lepton and heavy flavor identification at high luminosity and full event reconstruction at lower luminosity.

- Large acceptance in pseudorapidity η^2 with almost full azimuthal angle ϕ coverage everywhere.

- A highly efficient trigger system for most physics processes at the LHC.

2.3 The ATLAS Detector

ATLAS will be a general purpose detector, designed to exploit the full physics potential of the LHC. It is being constructed by a collaboration of 140 institutions in 34 countries. Figure 2.5 shows the global layout of the detector.

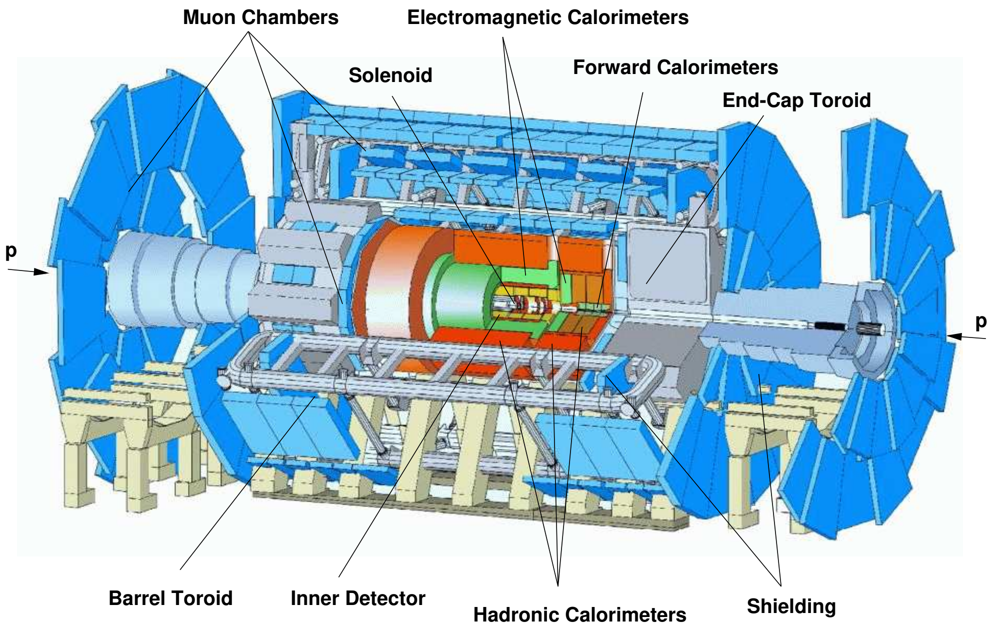


Figure 2.5: The ATLAS detector [12].

2.3.1 The Inner Detector

The Inner Detector is located in the center of ATLAS, aligned along the beam axis. It is cylindrically shaped with a diameter of 2.3 m and a length of 7 m. The task of the Inner Detector is to reconstruct tracks and vertices of events with high resolution. The layout of the detector is shown in Figure 2.6. At the inner radii it uses high resolution detectors. The highest granularity is achieved around the vertex region, where semiconductor pixel detectors are used. Surrounding the pixels are silicon microstrips. Due to their high cost, the number of precision layers must be limited. Straw tube trackers are therefore attractive in that they provide continuous track-following. The Inner Detector covers the

[2] pseudorapidity is defined as $\eta = -ln(\frac{tan\theta}{2})$, where θ is the polar angle. η is used instead of θ, as differential rapidity is invariant under change of the reference frame along the z-direction (beam axis).

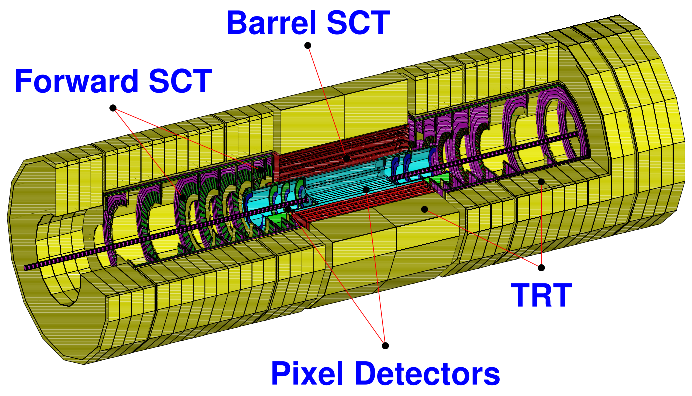


Figure 2.6: The Inner Detector of the ATLAS experiment [13].

pseudorapidity region from -2.5 to 2.5 and is contained in a solenoidal magnetic field of two tesla.

2.3.2 Calorimetry

The Calorimeter plays a central role in the ATLAS project, as many important physics processes require the identification and energy measurement of electrons, photons, jets and missing transverse energy E_T^{miss}. The ATLAS Calorimetry provides the means to these

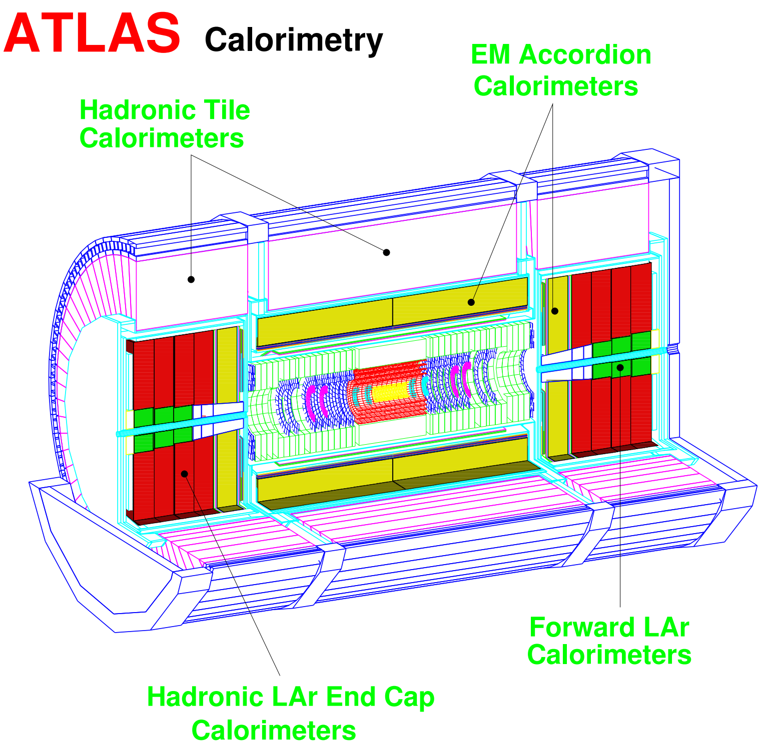


Figure 2.7: The ATLAS Calorimetry. [12]

tasks in a region of η from -4.9 to +4.9. Different types of calorimeter technologies are used in ATLAS in order to withstand the high radiation and to achieve high resolution. The common concept is that they are all of the sampling type, where layers of absorber material and sensitive material alternate. A cut-away view of the ATLAS Calorimetry is shown in Figure 2.7.

A cryostat surrounding the Inner Detector contains the Barrel Electromagnetic Calorimeter. Two end-cap cryostats enclose the Electromagnetic and Hadronic End-cap Calorimeters, as well as the Forward Calorimeter. All these calorimeters are of the liquid argon type, using liquid argon as the sensitive medium. This is due to it's tolerance to intense radiation and good insulating properties as well as the very low probability of electron capturing which would spoil the energy measurement.

The three cryostats are surrounded by the Hadronic Calorimeter which is divided into a barrel and two extended barrel sections. It uses scintillating plates of plastic as the sensitive medium and iron as the absorber material. Geometrically the Hadronic Calorimeter surrounds the Electromagnetic Calorimeter. Hadrons with their high mass pass the Electromagnetic Calorimeter without loosing much energy due to bremsstrahlung and only get absorbed in the absorber materials of the Hadronic Calorimeter in strong interacting processes. The absorber materials with a high cross-section for these strong interacting processes are copper, tungsten and iron. Table 2.2 gives a summery of the ATLAS Calorimetry including coverage, absorber and sensitive material and number of read out channels. According to their different specialties, several unique calorimeter

Calorimeter	$\lvert\eta\rvert$	**Absorber/Sensitive Medium**	**No. of channels**
E.M. Barrel	0-1.4	Pb/liquid Ar	128 000
Had. Barrel	0-1.0	Fe/scintillator	27 000
Ext. Barrel	1.0-1.6	Fe/scintillator	4 000
E.M. End-Cap	1.4-3.2	Pb/liquid Ar	82 000
Had. End-cap	1.5-3.2	Cu/liquid Ar	8 800
E.M. Forward	3.0-4.9	Cu/liquid Ar	6 060
Had. Forward	3.1-4.9	W/liquid Ar	7 070

Table 2.2: Summary of the ATLAS Calorimetry.

geometries are used in the ATLAS detector. The Electromagnetic Barrel and End-cap use lead plates formed in an 'accordion' shape as an absorbing material. These allow readout towers to point towards the interaction region.

The Forward Calorimeter uses a matrix of rods and tubes in order to achieve a very thin liquid argon gap, needed to achieve a short drift time in the gap.

In the Hadronic Barrel Calorimeter (Tile Calorimeter) the scintillating tiles are placed in planes perpendicular to the particle direction and staggered in depth. This provides good sampling homogeneity.

2.3.3 The Muon Spectrometer

The Muon Spectrometer surrounds the ATLAS Calorimetry with a total area of about 12000 m^2 of tracking chambers. It is based on the magnetic deflection of muon tracks in a magnetic field. A large superconducting air-core toroid magnet in the barrel and two smaller end-cap magnets inserted into both ends of the barrel toroid provide the necessary magnetic field for the bending of the tracks. For precision measurements of muon tracks, magnetic field Monitored Drift Tube (MDT) chambers are mainly used. Only in the high flux inner radii of the end-cap, Cathode Strip Chamber (CSC) are installed instead. As

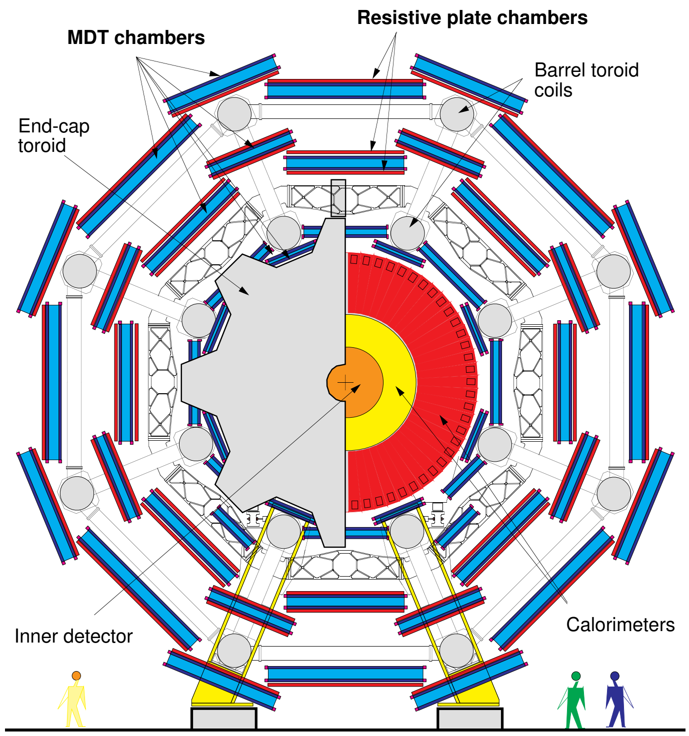


Figure 2.8: The ATLAS Muon Spectrometer [14].

the Muon Spectrometer is instrumented with separate triggering two types of triggering chambers are inserted. In the barrel there are three stations of Resistive Plate Chambers (RPC) and in the endcap Thin Gap Chambers (TGC) are installed for the sole purpose of triggering. Figure 2.8 shows a cut-away view of the Muon Spectrometer.

Chapter 3

The ATLAS Trigger System

3.1 Overview of the Trigger Concept

The whole ATLAS detector has approximately 147 million detector read-out channels. This makes for an enormous data volume for each event. Table 3.1 lists the numbers of read-out channels of the sub-detectors, alone with their corresponding event sizes. The table indicates that per event, 1.28 MBytes of data are obtained. With a bunch-crossing

Detector part	**Number of channels**	**Amount of data [kByte]**
Pixel detector	140×10^6	50
Tracker	5.6×10^6	850
Calorimeter	0.23×10^6	180
Muon Spectrometer	1.3×10^6	200
Total amount	147.13×10^6	1280

Table 3.1: Amount of data produced each bunch-crossing in the ATLAS sub-detectors [15].

rate of 40 MHz, the total data volume amounts to 51.2 TByte/s. It is clear that this amount of data cannot fully be read-out for off-line analysis. For this reason, an online trigger system is used to reduce the amount of data, keeping significant events and discarding unimportant ones.

The ATLAS trigger and data-acquisition (DAQ) system is based on three levels of event selection [16]. Each trigger level refines decisions made at the previous level. At full luminosity, an average of about 23 interactions will occur in each bunch-crossing every 25 ns. This results in an interaction rate of about 10^9 Hz. As the rate of selected events must be reduced to about 100 Hz for permanent storage, this requires an overall rejection factor of 10^7 for all trigger levels.

Figure 3.1 illustrates the data flow from the detector to the off-line storage. The vertical path corresponds to the data with finer granularity from the detector. After each trigger level, this data is reduced. As the decisions, on what data to keep or not, on Level-1 must be reached within 2 μs, Level-1 uses coarser granularity for the calorimeter

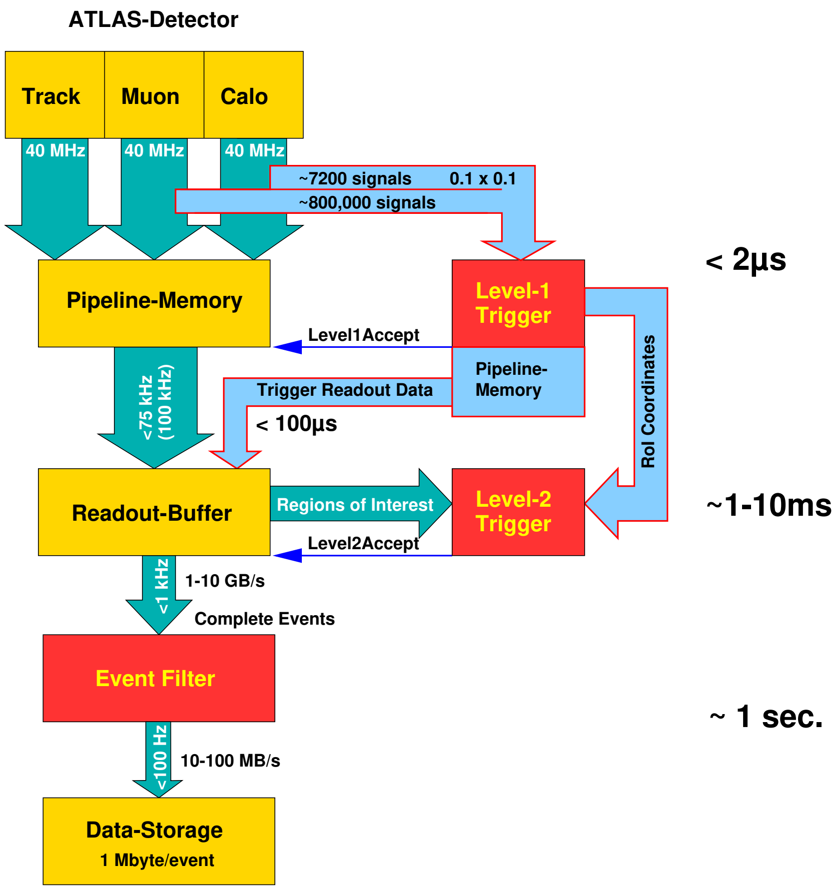


Figure 3.1: Detector read-out and trigger system [9].

signals and only a subset of the detectors in the muon system (RPC chambers in the barrel and TGC chambers in the end-cap). The short latency of 2 μs is necessary to keep the pipeline memory where the data is stored while the trigger reaches its decision, short and affordable. Level-1 reduces the event rate to below 75 kHz, upgradable to 100 kHz.

All the detector data for the bunch-crossing selected by Level-1 are then held in read-out buffers (ROBs). It remains there until it is either rejected by Level-2, at which point it is discarded, or it is further transferred to the Event Filter, the third level of event selection. Level-2 uses region-of-interests (ROI) information. This includes positions of interesting objects, which is directly provided by Level-1. Using this information means, that Level-2 selectively accesses data from the ROBs, taking only the data that are required to make the Level-2 decision. This second level of event reduction leaves an event rate of below 1 kHz.

After Level-2 the Event-Builder reconstructs physical events with the full granularity and resolution. In doing this, it uses similar algorithms which are used later on in the off-line analysis. It also makes possible another reduction in the event rate to a maximum of 100 Hz. This amounts to a data rate of about 100 MByte/s which is then stored permanently.

3.2 The Level-1 Trigger

The Level-1 Trigger system is composed of a number of building blocks - the Calorimeter Trigger, The Muon Trigger and the Central Trigger Processor (CTP). The trigger algorithms search for signatures involving isolated electrons, photons, hadrons and taus, jets, muons and calculate the global energy sum of the calorimeter, to be sensitive to missing E_T. All trigger algorithms are implemented in dedicated hardware chips where both Application-Specific-Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) are used to meet the stringent latency criteria of 2 μs, in which the Level-1 decision has to be reached. This is why the Level-1 trigger is also often referred to as a 'hardware trigger'.

3.2.1 The Calorimeter Trigger

The input to the Level-1 Trigger is for the calorimeter part based on reduced granularity. Analog calorimeter signals are summed to 'trigger towers' on a basis of a two dimensional grid with steps of 0.1 in the η and ϕ direction. This is done separately for the Electromagnetic and the Hadronic Calorimeter. It amounts to about 7200 signals which are then transmitted electrically through twisted pair cable to the Level-1 Calorimeter Trigger. There, the trigger-tower signals are digitized using a dedicated analog-to-digital converter system. Digital signal processing is then applied to extract the deposited transverse energy for the calorimeter pulses and to assign it to the correct bunch crossing. This is necessary, since the calorimeter pulses extend over several bunch-crossing periods. This section of the Calorimeter Trigger is labelled as Pre-Processing in Figure 3.2 and will be discussed in detail in the next chapter.

The following processing in the Calorimeter Trigger is fully digital and is divided into two parallel working parts, the Cluster Processor and the Jet/Energy-Sum Processor. The Cluster Processor (CP) will make use of an electron/photon and an hadron/tau algorithm which will perform a search for electrons/photons and hadrons/taus with high transverse momentum or dedicated multiplicity, which then are referred to as objects. The Jet/Energy-Sum Processor (JEM) searches for jets with high transverse energy and calculates the total transverse energy E_T and the missing transverse energy E_T-miss.

The electron/photon algorithm will search for trigger tower cells with a transverse energy E_T deposition, which is greater than a given threshold and is 'isolated'. Therefore, there are sets of thresholds that can be programmed, each consisting of a threshold on the E_T of the cluster, an isolation threshold of the surrounding deposited E_T in the Electromagnetic Calorimeter and a threshold on the E_T in the corresponding Hadronic Calorimeter tower, which can veto the decision if a deposition would occur there. The isolation criteria is fulfilled when E_T in a ring of neighboring trigger-tower cells is smaller than a given threshold. In the same way, there are sets of thresholds for the hadron/tau algorithm, now with an isolation threshold for the surrounding E_T in the Electromagnetic *and* the Hadronic Calorimeter, as hadrons and taus are producing showers in both calorimeters. The jet algorithm is looking for passed thresholds of transverse energy depositions in the Electromagnetic and Hadronic Calorimeter, which have been summed together in the Pre-Processor to so-called 'jet-elements'. As jets are extended objects,

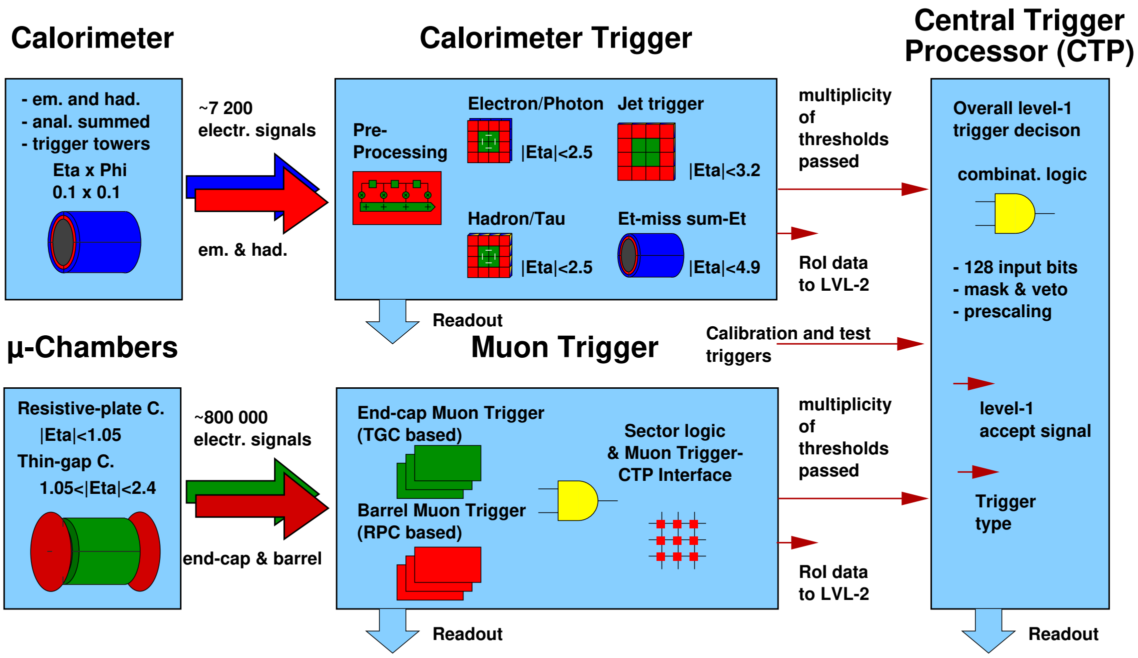


Figure 3.2: Overall Level-1 Trigger system architecture. [9]

the algorithm is applied to quadratic windows which combine several jet-elements. For the jet algorithm there are eight programmable thresholds. The size for the jet-window is programmable. This is important, as as an under-sized window would not contain the full jet, and one that is too big would add noise and pile-up over the larger area which will decrease the resolution. To calculate the total E_T and E_T-miss, a summation is performed over all the trigger towers. Eight thresholds can be applied to the E_T-miss trigger and four to the total E_T trigger. Figure 3.2 shows the coverage in pseudorapidity to the corresponding algorithm. For the E_T-miss trigger, it is important to include a large acceptance in pseudorapidity to avoid wrong triggers caused by objects like highly longitudinal jets which just have not been ‘seen’ by the detector.

The multiplicities of thresholds which have been passed for all the different objects are then transmitted to the Central Trigger Processor. The coordinates of where objects have been found are sent as ROI data directly to Level-2.

3.2.2 The Muon Trigger

The input to the Muon Trigger comes from the muon trigger chambers, namely the RPC and the TGC detectors. These are a subset of the overall muon chambers especially designed for triggering purposes. There is a total of more than 800 000 input signals to the Muon Trigger coming from the RPC and TGC front-end electronics. The trigger has to identify the bunch-crossing that contained the muon and search for patterns of hits in the trigger chambers, consistent with muons with high transverse momentum coming from the interaction region. Therefore the Muon Trigger measures the trajectory for muons with high transverse momentum. As indicated in Figure 3.2, the Muon Trigger is subdivided into a part specific to the RPC chambers, another part to the TGC chambers and a part that combines the information from the full system and calculates the results. The trigger algorithm provides six programmable p_T thresholds. The multiplicity of muons for each of the six thresholds is then passed to the CTP. Also similar to the Calorimeter Trigger, ROI data is sent directly to the Level-2 Trigger.

3.2.3 The Central Trigger Processor

The role of the Central Trigger Processor (CTP) is to combine the information from the Calorimeter Trigger and the Muon Trigger regarding the different object types, and then to make an overall Level-1 accept or a reject decision. This is achieved with trigger menus programmable with up to 96 items, where each item represents a combination of requirements on the input data. An example of this could be, that at least one electron has occurred which passed a certain threshold occurring together with an E_T-miss above another specified threshold but no muons with high p_T.

The CTP will generate a Level-1 accept signal, if any of the 96 menu items is satisfied. These Level-1 accept signals, the trigger type information, the bunch-crossing number and the event number are then distributed via the Timing, Trigger and Control system (TTC) to the read-out and the front-end electronics.

Chapter 4

The Level-1 Calorimeter Trigger Pre-Processor

The last chapter gave an overview of the Level-1 Trigger, with its major building blocks. In this part, there will be a focus on the Pre-Processor system of the Calorimeter Trigger. The arrangement within the Calorimeter Trigger was already shown in a general overview, but will be now explained in greater detail.

The input to the Pre-Processor are all the pre-summed trigger towers with a coarser size of 0.1 x 0.1 in η and ϕ coming from the calorimetry. The output of the Pre-Processor are sent via high speed serial links to the subsequent Cluster Processor and Jet/Energy-Sum Processor of the Calorimeter Trigger. This is illustrated in Figure 4.1. As the Cluster Processor and the Jet/Energy-Sum Processor work parallel, both processors have to be supplied with data at the same time. For the Cluster Processor this data has a granularity of 0.1×0.1 in the $\eta \times \phi$ plane, and a reduced granularity of 0.2 x 0.2 for the Jet/Energy-Sum Processor. Another duplication of specific data results from the mapping of trigger tower signals in bunches of ϕ-quadrants into electronic modules. The signals at the ϕ-edges are needed to be duplicated, as the subsequent processor algorithms need these signals for their individual, parallel working, algorithms. This duplication is referred to as 'fan-out'.

4.1 The Tasks of the Pre-Processor

The Pre-Processor is performing its tasks at a very responsible position, as *all* the trigger tower signals from the calorimeters have to go through it. This requires, that Pre-Processor components are easily and fast repairable, to ensure effective data taking and a minimum of downtime. This can be achieved with two considerations.

1. to use identical modules with the same functionality, to avoid needing different types of spare modules.

2. to implement major tasks in easily exchangeable smaller units, where no time-consuming soldering is involved. - Both requirements are fulfilled in the Pre-Processor.

The tasks of the Pre-Processor can be divided into two major blocks. The one is the processing of the real time data path, coming from the calorimeters and going to the

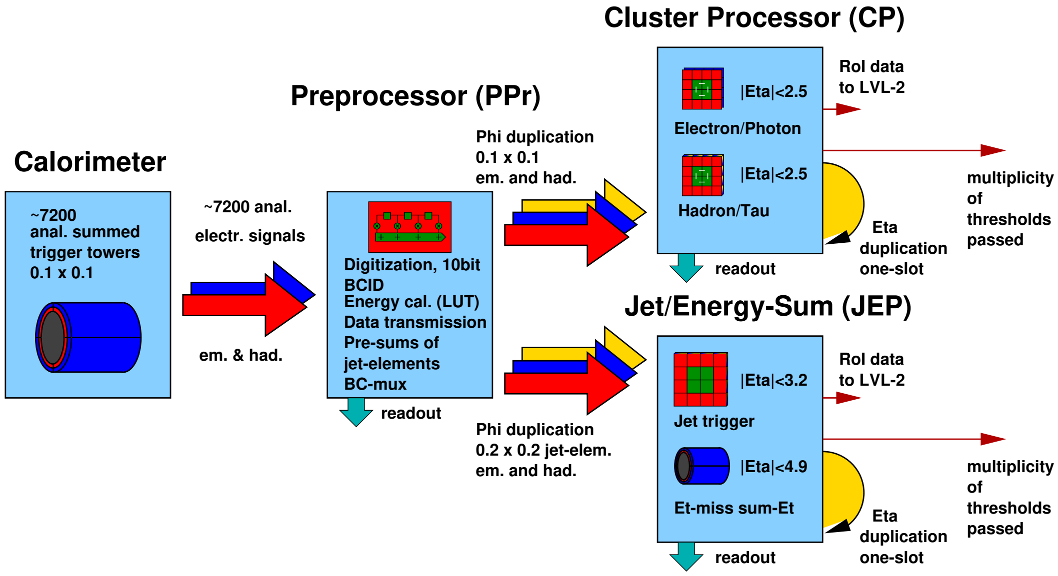


Figure 4.1: Level-1 Calorimeter Trigger system architecture. [9]

subsequent processors. The second one is the read-out of raw trigger data, to check the overall trigger performance. The following list will summarize these tasks:

Preprocessing Tasks

- **Reception of analog trigger tower signals:**
  The differential analog trigger tower signals are received by a line receiver circuit, which adjusts the zero baseline for each input signal using a 6-bit digital to analog converter (DAC) and transforms the differential signal to a unipolar signal.

- **Digitization of analog trigger tower signals:**
  Each analog trigger tower signal will be digitized to 10-bit resolution, using a dedicated analog-to-digital converter (ADC). For this task, the AD9042 from Analog Devices [17] will be used.

- **Phase adjustment and synchronization:**
  Because of the different values of time-of-flight delays for the particles from the interaction point to the calorimeter and different length of cables from the detectors to the trigger cavern, it is necessary to synchronize the data to the same bunch-crossing. This is done by a FIFO (first in first out), implemented in the PPrASIC[18], which can delay signals in steps of 25 ns. The fine adjustment in steps of 1 ns is done by an ASIC called Phos4 [19] which has been developed by the CERN Microelectronics group. This synchronization will allow to digitize the input signal at its maximum and to synchronize the signals to the right bunch-crossing in time.

The following three tasks, are implemented in the PPrAsic which will be addressed in the second part of this chapter.

- **Bunch-crossing identification (BCID):**
  Two algorithms identify the transverse energy deposition to the corresponding bunch-crossing in time. One algorithm is applied to non-saturated signals and the other one to saturated signals above 250 GeV.

- **Energy calibration:**
  A lookup table (LUT) is used to calibrate the digitized data to the deposited transverse energy E_T. It maps the 10-bit data to 8-bit with a least significant bit (LSB) of 1 GeV.

- **Formation of jet elements:**
  Four 8-bit trigger towers are pre-summed to jet-elements with a granularity of 0.2 $\times$ 0.2 in η and ϕ. This is done separately for the electromagnetic and hadronic calorimeters, to allow possible separate jet thresholds in the Jet/Energy-Sum Processor.

- **Serial data transmission:**
  The pre-processed data are sent to the subsequent processors via high-speed serial links, to limit the number of connections. For this, LVDS[1]-links from National Semiconductor [20] are used.

Read-Out Tasks

- **Read-out of raw trigger data:**
  To check the overall trigger performance, raw trigger data is read-out. This allows to reconstruct on what the trigger decision was based on. For this a RemFPGA[2] will be used to collect the data from the PPrAsics. A Read-Out Driver module [21] collects data from the RemFPGAs, via a parallel PipelineBus.

- **Histogramming:**
  The trigger performance will be monitored by a histogramming feature. This will for example allow to monitor the E_T spectrum of the raw ADC data or the calibrated output after the look-up table.

4.2 Hardware Components of the Pre-Processor System

The Pre-Processor consists electronically out of 128 identical Pre-Processor Modules (PPMs). 16 Read-Out Driver Modules collect the read-out of the PPMs via a ring-like bus, called PipelineBus on the backplane and send the read-out data via S-Links (CERN standard links)[23] to the Read-Out Buffers (ROB's). These modules fill eight crates which are hosted in four racks. Each crate hosts additionally eight VMEbus Crate Controllers for VME access to the different modules. As the overall Level-1 decision has to be made within 2 μs, which is equivalent to 80 bunch-crossings, the Pre-Processor has a fixed latency of 18 bunch-crossings to complete its tasks. This puts stringent requirements on the used

[1] Low Voltage Differential Signaling
[2] RemFPGA: Read-Out Merger FPGA

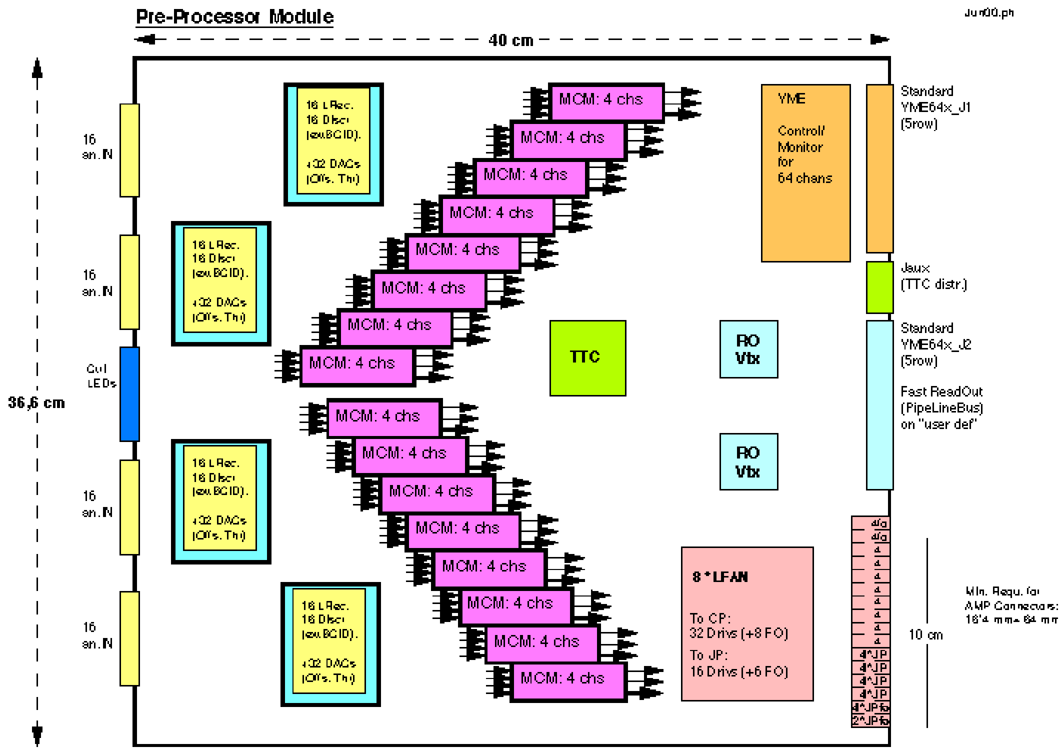


Figure 4.2: First layout of the Pre-Processor Module. [22]

components. Therefore a fast system with high integration density is required. This can be achieved using Multi-Chip Module technology. This means, that the pre-processing stages for a limited number of channels are performed on one multi-layered printed circuit board, where components in 'die'[3]-form are grouped together. The Pre-Processor Multi-Chip Module (PPrMCM)[22] contains all the pre-processing stages for four trigger tower signals on an area of 14 cm^2. It is also the smallest exchangeable unit on a Pre-Processor Module.

A Pre-Processor Module is a Printed-Circuit-Board (PCB) and processes 64 channels, thus has to carry 16 PPrMCMs, which form the core of the module. Figure 4.2 shows a first layout of a PPM. The module will be 9U[4] high and 40 cm in depth. Four input connectors, each handling 16 differential analog signals, will be located at the front panel. Between the front panel and the PPrMCMs, there will be four differential line receiver boards which each processes 16 differential input signals and send them further to the PPrMCMs. The position of the 16 PPrMCMs has been optimized in terms of good heat exchange and to minimize crosstalk between the analog inputs and the high speed differential outputs. A temperature simulation of different configurations of the PPrMCMs on a PPM will be presented in Chapter 8.1. The two boxes labelled 'Vtx' represent the RemFPGA, which will collect all the read-out data from PPrMCMs and make them

[3]die:die means generally a silicon chip without the packaging around it
[4]9U:U means unit, used in VME specifications. 9U=36.6 cm.

available at the PipelineBus interface on the backplane. There will also be LVDS driver chips located near the backplane of the module, which buffer the LVDS signals coming from the PPrMCMs and send them to the Cluster Processor and Jet/Energy-Sum Processor modules via twisted pair cables.

4.2.1 The Pre-Processor Multi-Chip Module

The functionality of the Pre-Processor Multi-Chip Module is shown in a block diagram in Figure 4.3. It will consist of 9 dies and be manufactured in a laminated MCM-L process using four routing layers to make the necessary connections between the components. As

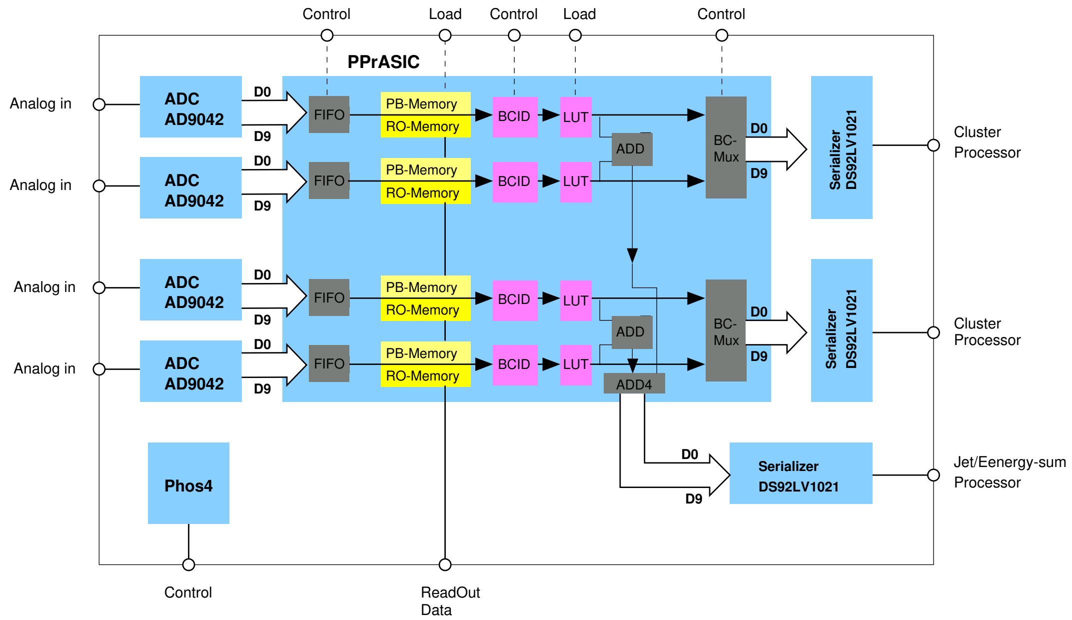


Figure 4.3: Block diagram of the Pre-Processor Multi-Chip Module. [22]

shown in the block diagram, four AD9042 chips are used to digitize four input channels. The output of the four ADCs are input to the PPrAsic which processes four channels in one chip. The Phos4 chip is needed to adjust the phase of the clock input of the ADCs so that the peak maximum of the input signal can be digitized. Three LVDS chips will serialize the output of the Pre-Processor to a data rate of 480 MBit/s differential output per LVDS.

The developments towards a final PPrMCM will be the focus of the following chapters. The next chapter will give an overview of the manufacturing technology as investigated for the demonstrator Multi-Chip Module. In Chapter 6 and 7, evaluations for the PPrMCM and the used components will be presented. Chapter 8 will then summarize all these developments in a first layout and description of the PPrMCM and show results on thermal simulations.

4.2.2 The Pre-Processor ASIC

The Pre-Processor ASIC is designed in Verilog HDL[5] and will be produced in a $0.6\mu m$ CMOS[6] process offered by Austria Micro Systems (AMS). The PPrAsic does all the digital pre-processing for four trigger towers. The block diagram in Figure 4.3 shows the most important building blocks, where most of them were already briefly described in Section 4.1. These building blocks are: The FIFO circuit, the playback and read-out memory, the BCID algorithms, the look-up table (LUT), the formation of jet elements and bunch-crossing multiplexing.

The FIFO circuit synchronizes the data from the ADCs to the right bunch-crossing. This is done by storing the data in a memory for as long, until the delay due to cable lengths or time-of-flight from the interaction point to the different detectors, has been compensated.

Two types of data can be read out of the PPrAsic via a serial interface. Raw digitized data from the ADCs and as the second type, BCID results including the calibrated transverse energy. The data to be read out is stored in two separate pipeline memories. The length of the pipeline is 128 words, which is equivalent to a time of 3.2 μs. The playback memory is also accessible via the serial interface and can be used to inject data for technical tests of the trigger system.

The bunch-crossing identification is done by two different algorithms. One is optimized for non-saturated pulses, and the other one is optimized for saturated pulses above this value. Both algorithms are implemented in parallel and are always active. A decision logic decides which of the algorithms is used for the final result.

A look-up table is used to fine calibrate the digitized data to the deposited transverse energy. The incoming ADC data, which are 10-bit wide words, are mapped to 8-bit. This can be done by using a 1024*8-bit wide memory. The look-up table can also be used to subtract a pedestal and it can apply a threshold to suppress noise.

The Pre-Processor sums four trigger towers to jet elements, which have a size of 0.2×0.2 in $\eta \times \phi$. This requires, that all four inputs to a jet element must be adjacent trigger tower channels. The 10-bit sum is truncated to 9-bit before transmission.

Bunch-crossing multiplexing is a transmission scheme which allows to double the bandwidths of the serial links to the Cluster Processor. The scheme is, that the content of two channels, which occurred in the same bunch-crossing, are sent in two consecutive clock cycles to the Cluster Processor rather than synchronous. Therefore a flag bit is added to provide information to the receiver, so that it can definitely identify the bunch-crossing to the corresponding channel content.

For a more detailed description of the Pre-Processor Asic please see the PPrAsic User and Reference Manual [18].

4.2.3 The Read-Out Merger FPGA

One or two RemFPGAs will be located on a Pre-Processor Module. 16 serial interfaces will connect the RemFPGA with the 16 PPrAsics on one PPM. If an overall Level-1 accept

[5]HDL:Hardware Description Language
[6]CMOS:Complementary Metal Oxide Semiconductor

decision has been reached by the Central Trigger Processor, the RemFPGA will collect all the read-out data from the PPr-Asics and store it in internal memories. To reduce the data rate, a compression algorithm is applied to the data, which will reduce the data by a factor of about 2.3. This data will then be collected by the PipelineBus.

This data link is also used to configure the PPrAsics. There the configuration data can originate either from the VME crate controller via the VMEbus interface or from the Read-Out Driver via the PiplineBus to the RemFPGA, which then send the configuration data to the PPrAsic's.

4.2.4 The Read-Out Driver

The PipelineBus connects eight Pre-Processor Modules to one Read-Out Driver Module to a ring-like bus. Figure 4.4 shows a schematic view of this set-up. One Read-Out Driver collects thus all the read-out data from the RemFPGA's on the eight PPM's. The collected data is then transmitted via a standard S-Link[23] to the ATLAS data acquisition system (DAQ). The Read-Out Driver will be implemented in an FPGA using Verilog HDL to implement the necessary functionality.

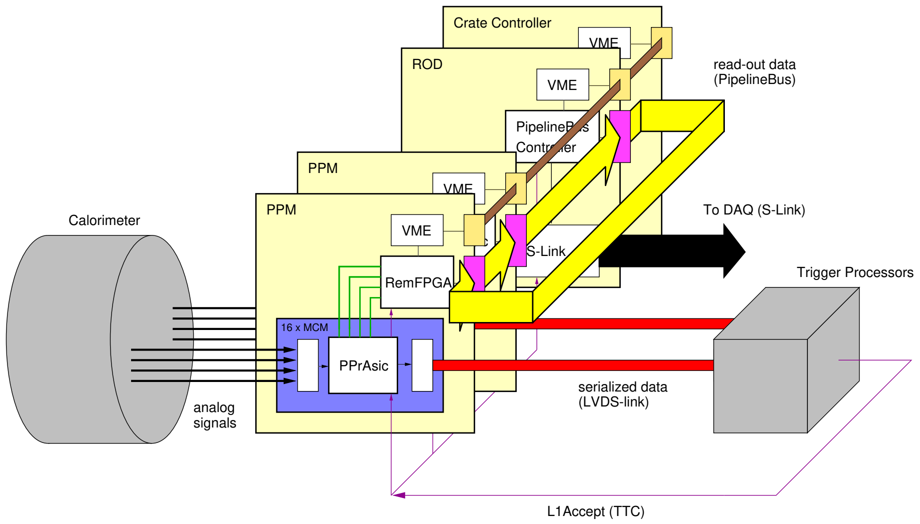


Figure 4.4: Block diagram of the read-out configuration. [24]

Chapter 5

The Demonstrator Multi-Chip Module

To establish MCM design techniques and experience for the final Pre-Processor, a demonstrator Multi-Chip Module (PPrD-MCM) has been built. The aim of this project was to investigate a suitable MCM packaging technology which has similar functionality as to the final PPrMCM. As a result, the MCM had to include the pre-processing and the readout for four trigger tower signals in a compact layout. Please see [9] for a detailed description of the design and manufacturing process.

5.1 Functional Description

The use of Multi-Chip Module technology for an electronic system has a lot of advantages. To assemble many chips in a single package reduces system size and external connections. It therefore also minimizes run-time between the components, as input and output connections between chips are used as one-to-one connections. This has practical advantages such as avoiding long wide buses between spread components. Only signals like control, power supply the input to the package and the output of the package have to be transmitted. All the processing is done internally.

The demonstrator Multi-Chip Module consists of nine dies. Two dual flash ADCs from Analog Devices [26] with 8-bit resolution, four FeAsics [27], a PPrAsic prototype which does all the processing for one channel, the Finco Asic [9] and two gigabit transmitters from Hewlett Packard [28]. Figure 5.1 shows the demonstrator Pre-Processor Multi-Chip Module. The signal flow is from left to right. The two dual flash ADCs perform the digitizing to 8-bit precision for the four analog trigger towers at the input. 'Flash' means that only one clock cycle (25 ns) is needed for the digitizing. A dual flash ADC has the advantage that the number of analog components and the total number of dies is reduced. The four 8-bit data buses are then each digitally processed by an FeAsic. The Flip-chip INterCOnection Asic (FINCO) has been designed specifically for the demonstrator MCM. Its task is to multiplex data from the four FeAsics from 40 MHz to 80 MHz, to adjust the baseline of the analog input signals with the use of a 10-bit digital-to-analog converter

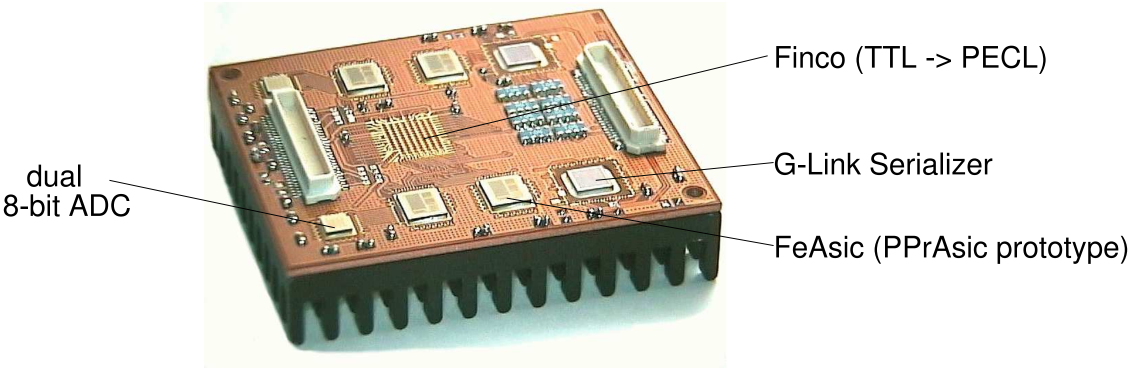


Figure 5.1: The demonstrator Multi-Chip Module [9].

(DAC) and to convert the FeAsics TTL[1] outputs into PECL[2]-levels. This is necessary, since the G-link dies have no TTL inputs. The converted data coming from the Finco Asic are then serialized by the two G-links to an eligible data rate of either 800 MBits/s or 1.6 GBits/s. The latter one is only possible when the multiplexing mode of the Finco Asic is used. In that case, only one G-link set is necessary to transmit the data output from the four FeAsics.

5.2 Technology Overview

Except the Finco Asic, all dies are used chip-on-board (COB) on the MCM substrate. This means, that the silicon die is glued directly onto the MCM substrate. The connection between the substrate pads and the pads on the chip is performed with a 25 μm thick aluminum wire, which is bonded onto the pads, using a standard ultrasonic wire-bond technique. Figure 5.2 shows a G-link chip after bonding. For the Finco Asic, flip-chip

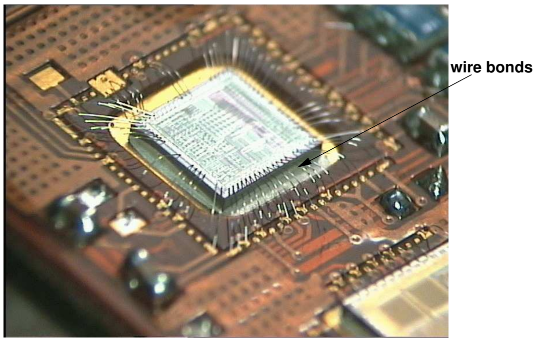


Figure 5.2: A G-link die with bond connections. [9].

mounting has been used. In this technique, the silicon die is turned upside-down and

[1]TTL:Transistor Transistor Logic
[2]PECL:Positive Emitter Coupled Logic

small solder bumps of 300 μm in diameter are used to form the electrical contacts between pads on the chip and bonding pads. In Figure 5.1, the Finco Asic has not been soldered on yet. This makes the two dimensional pad array for the solder bumps visible.

5.2.1 MCM Layer Structure

The substrate of the PPrD-MCM has been produced based on a laminated multi-layer printed circuit board (PCB) technology. In this technology, the structures of the layers are formed by etching patterns into copper foils. The copper foils are laminated onto a polyimid insulator material. The interconnection between these copper layers are performed with electroplated vias. For the PPrD-MCM, special plasma etched micro-vias have been used which allow via sizes of down to below 100 μm.

A four routing layer design has been chosen for the PPrD-MCM. One layer has been used as a universal ground plane, one layer each for routing in the x and y direction and the fourth layer is the top layer, which mainly hosts the dies, connectors, resistors and capacitors. 5.3 shows a cross-section of the layer structure of the PPrD-MCM. One

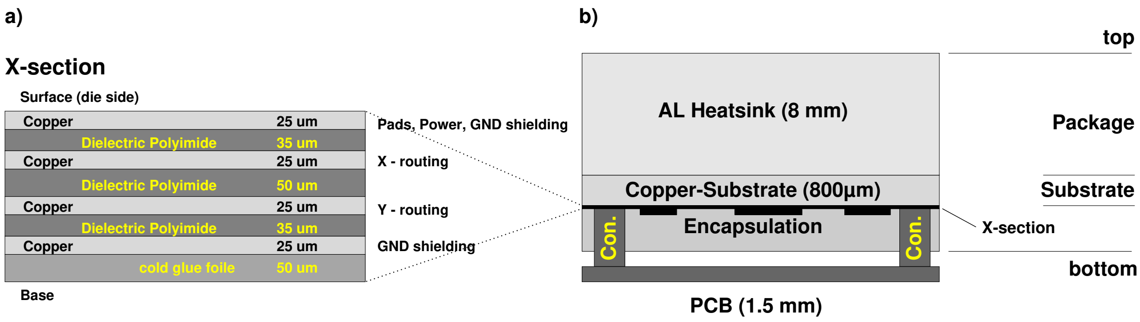


Figure 5.3: a) shows the cross section of the layer structure and in b) the whole stuck-up of the MCM is illustrated. [9].

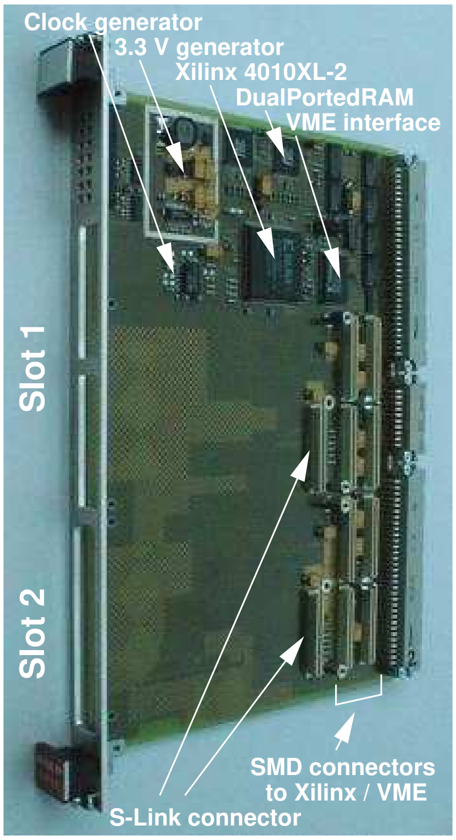
laminated layer is 50 μm thick and consists of a copper foil and an insulating polyimid material both 25 μm thick. These layers are then glued together with an epoxy glue approximately 10 μm thick. As the core polyimid foil has double the thickness, the total width of the layer structure amounts to 220 μm. The four layers are then mounted on a rigid copper base of 0.8 mm, which is attached to an aluminum heatsink.

As the used ADCs and the G-links have a high power consumption of about 1 Watt and 2 Watt respectively, special techniques are applied to provide good thermal conduction. In the case of the ADCs, so-called thermal vias have been used. These are vias which connect through the whole cross-section to the ground plane. For the G-link dies, a cut-out through the four layers of an area slightly larger than the chip allows one to glue the chip directly onto the rigid copper substrate. These methods result in very good thermal conduction. This is essential due to the exponential dependency of the component failure rate with temperature.

5.3 The PPrD-MCM within the Pre-Processor Test System

The Test System of the Pre-Processor is a down-scaled version of the full Pre-Processor system. It allows to test and to develop prototype components of the Pre-Processor. The flexibility of the system allows stand-alone tests of the individual components, but also configurations, where communication between different modules are investigated. The Test System consists of general purpose motherboards and several daughterboards, which provide the special application specific functionality. The daughtercards are designed obeying an underlying CMC[3] standard, defined by the IEEE[4].

5.3.1 The General Purpose Motherboard



The general purpose motherboard functions as a CMC card carrier. It is a 6U (23.3 cm in height) VME[5] module with two slots for two CMC daughtercards. A FPGA on the motherboard gives the possibility to control the daughtercards by programming a specific FPGA design to the corresponding CMC cards.

A dual-ported RAM[6] with 32 KByte in size, accessible from the FPGA and a VME interface, gives one the possibility to read and write data into a memory from both sides. An on-board clock generator provides two independent clocks in a frequency range of 0.4 - 120 MHz.

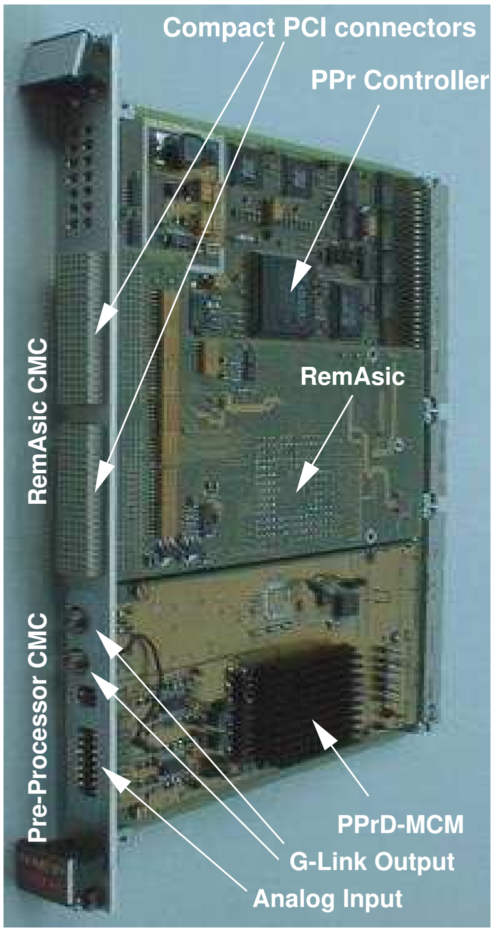
Two supply voltages are available for the CMC daughtercards on the corresponding connectors, 5 V and 3.3 V. The latter is generated on-board.

Eight SMD connectors are provided according to CMC specification. Most of those pins have connections to the motherboard FPGA, the VME-interface and between eachother. Two more connectors are compatible with CERN's Standard-link (S-link) specification.

There are nine daughterboards available: A Master-CMC, a General I/O-CMC, a Rem-Asic-CMC, a ROD-CMC, a SLink-CMC, a LVDS-CMC, a GLink-CMC, an ECMC, which will be the focus of the next chapter and a Pre-Processor-CMC, which hosts the PPrD-MCM. For every configuration with application specific daughtercards, the unit out of motherboard and one or two daughterboards gets a different identity.

[3]CMC:Common Mezzanine Card
[4]IEEE:Institute of Electrical and Electronics Engineers
[5]VME:Versa Module Eurocard
[6]RAM:Random Access Memory

5.3.2 The Pre-Processor Unit



This unit consists of one motherboard, which carries a Rem-Asic-CMC in the first slot and a Pre-Processor-CMC in the second one. It has the functionality of a Pre-Processor Module (PPM) for a reduced number of four channels, performing all pre-processing and read-out tasks. The Rem-Asic is a prototype chip which performs the read-out from the four FeAsics on the PPrD-MCM. It has been developed by the ASIC laboratory of the University of Heidelberg [29]. The final design of the read-out of the PPrAsics on the Pre-Processor Modules has been chosen to be implemented in a FPGA (RemFPGA) instead. This gives the flexibility to change the read-out functionality at a very late stage. The PPrD-MCM is located on the CMC card in the second slot connected via two connectors with 60 pins each. With this set-up all the pre-processor tasks can be tested in a stand-alone mode, where no interconnection between other motherboards via the PiplineBus is applied.

Measurement results for the pre-processing on the real-time data path, where two analog trigger towers are pre-processed and transmitted serially to a Glink receiver card, can be found here [9]. For measurements on the read-out with the RemAsic, please see [30].

5.3.3 The Assembly of the PPrD-MCM and Outcome

Six PPrD-MCM have been assembled for test purposes within the Test System. This involved chip mounting, chip bonding and soldering of SMD[7] capacitors, connectors and resistors. The flip-chip mounting of the Finco Asic has been done 'out of house' [31], as this requires very advanced machinery. Unfortunately the flip-chip mounting for these six MCMs was not very successful as later tests showed that several flip-chip pads had no connections.

The 'in house' assembly process has been chosen to be as follows:

1. Soldering of capacitors and resistors

2. Mounting of dies

[7]SMD:Standard Mounting Device

3. Wire bonding
4. Chip power-test
5. Soldering of connectors

Soldering of capacitors and resistors

The sizes of the used capacitors and resistors, where in SMD units 0402[8] and 0603 respectively. This requires a very thin soldering iron and tin-solder. The small sizes, require, that the soldering has to be performed with the help of a microscope. The reason why the soldering has been done prior to the chip mounting is to avoid solder splashes resulting from the soldering process to ruin the chips or bonding-pads.

Mounting of dies

The dies, which are used chip on board, have been mounted onto the substrate using a two component epoxy resin from EPO-TEC [32][33]. To obtain a uniform epoxy film a method has been used where basically a metal stamping tool is stamped into a film of epoxy, that is spread out evenly on a rigid surface. This stamping tool with the epoxy is then stamped onto the substrate. Figure 5.4 illustrates this method. The area of the

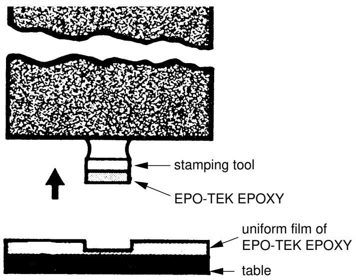


Figure 5.4: Stamping process for a uniform epoxy film [32].

stamping tool has been chosen slightly smaller than the chip area. A good contact to the chip is important for the thermal conductance as only the area which is covered by the epoxy can contribute to the thermal conductance. For the two dual ADCs, electrically insulating epoxy has been used, as the chip substrate rests on -5 V and the substrate area of the chip is grounded. The G-Links and FeAsics are glued on with electrically conductive silver epoxy.

The next step is a correct positioning of the chips onto the epoxy. This has been done with a suction pump. When all chips are placed, the epoxy needs to be hardened in an oven. A low temperature of 80°C has been chosen for 90 minutes, not to affect the chips.

[8] 0402:40×20 mills, size of SMD device

Wire-bonding

To connect the substrate pad to the chip pad an ultrasonic wire bonder has been used. The method is based on ultrasonic vibrations of a bonding needle which is placed onto a pad. The bonding wire is held inbetween. The fast movement of the needle heats the touching materials up and melts them together. The used bonding wire is made out of aluminum and is 25 μm thick. The pads on the substrate have a quadratic shape with 150 μm width. The bond pads on the chip surface is also a square and about 100 μm wide.

Sometimes it can happen, that the bond does not hold. If this happens, one can try to place a second bond if the remaining pad area allows that. The fraction of the number of pads which had to be bonded a second time divided by the total number of bonds is referred to as bonding yield. Table 5.1 shows the yields which were obtained out of assembling six demonstrator MCMs. The bonding yield for the FeAsics is lower than

Chip Type	Number of Bonds	Redone Bonds	Bonding Yield
FADC	504	2	99.60 %
FeAsic	1176	57	95.15 %
G-link	732	3	99.59 %

Table 5.1: Bonding yield according to chip type.

the one of the ADCs and the G-links. The reason for this is, that the chip pads of the FeAsics are not as rigid as the one from the ADCs and the G-links. This may be due to mis-adjusted process parameters of the chip foundry.

Chip power-test

After the chips have been bonded, a power test can be performed. There the supply voltages and the grounds are applied via needle probe holders. The corresponding current flow can be measured and compared with the chip specification. This allows a first identification of faulty chips if the measured current does not meet the specification. If a faulty chip is detected it can be exchanged by a new one.

This has been investigated with all three chip types. After locally heating up the chip with a soldering iron, the chip could be taken off with a tweezer. This technique becomes especially difficult for a G-link as through the used 'cut-outs' the chip is mounted on the rigid copper substrate with an area of the whole MCM and therefore high heat capacity.

Soldering of connectors

The two connectors had to be soldered onto the substrate at the very end, as they are placed very close to the ADCs. This caused, that the bonding needle could not reach the pad on the substrate for the ADC if the connector was already placed.

The experience gained from the assembly process has influenced the design of the final PPrMCM. The outcome and consequences are as follows:

Outcome and Consequences

- **MCM pads:** The pad size of $150\mu m \times 150\mu m$ on the substrate has been found to be too small for a possible necessary second bond. A rectangular shaped pad of $150\mu m \times 300\mu m$ will allow a second bond to be place behind the failed one.

- **Connector placement:** The connectors have to be placed away from the chips, where they cannot interfere with the bonding process.

- **Use of bond technology:** The difficulties experienced with flip-chip mounting is not encouraging to pursue further studies in this area. As the Pre-Processor is located at a very responsible position, the used technology should be well established. As wire bonding has been a standard technology for years, the PPrMCM will completely make use of this technique.

- **Chip pads:** Different chips show different rigidity of their chip pads. This has to be taken into consideration when choosing the process parameters for Asics but also when parameters for bonding machines are chosen.

- **Chip replacement:** As analog dies are difficult to test at full frequency, the percentage of faulty analog chips is higher compared to the packaged version. This makes the repair of a faulty MCM due to a broken chip necessary. A first simple method has been found with the use of a soldering iron, a more sophisticated is necessary, as the production of the PPrMCMs amounts to a total number of about 3300 pieces including spares.

This chapter discussed an existing prototype of a Pre-Processor Multi-Chip Module. For the final MCM some changes have been decided. This includes the change to higher digitizing precision from 8-bit to 10-bit. As no 10-bit flash ADC exists, a disadvantage for the higher precision will be, that the digitizing will add more to the overall latency.

Another change affects the serialization. The release of LVDS links with their low power of about 140 mW per chip and relatively low costs favors them against G-links with their high power consumption of up to 2 Watt. But due to their lower serial data rate of 480 MBits/s as compared to the maximal 1.6 GBits/s of a G-link, three LVDS serializers have to be used instead of one G-link.

To investigate the interplay of these new components and to evaluate layout properties an intermediate step between the demonstrator MCM and the PPrMCM has been inserted in form of an evaluation CMC-Card, called ECMC.

Chapter 6

The Evaluation CMC-Card (ECMC) for the PPrMCM

The evaluation CMC card (ECMC) hosts three of the four types of chips used on the final PPrMCM. Only the fourth type, the PPrAsic, is missing. The used chips are two ADCs, two LVDS chips and one Phos4. These chips are mounted onto the CMC-Card using a chip-on-board (COB) technique as is used on the MCM.

6.1 The Purpose of the ECMC

The ECMC uses three types of chips which will be on the final PPrMCM for the first time as dies[1]. Hence, the first important purpose to build the ECMC, is to gain experience with the interplay and use of these dies.

Another important purpose is aligned with the output stages of the ADC. The manufacturer of the ADC, Analog Devices, recommends that current limiting resistors should be applied at the ADC outputs. At first this does not seem to be a big issue, but that is not easily achievable on the MCM where limited amount of space is an issue. The 40 output resistors for the four ADCs would occupy an area of about 20 percent of the MCM. One should therefore evaluate whether or not output resistors on the MCM are truly a necessity.

For the design of the PPrMCM, the ECMC allows layout evaluations. This addresses the ground management and the footprints of the dies. A die footprint is the immediate surrounding of a chip, including the routing of signal and power tracks and the placement of block capacitors and additional needed components. Ground management is the handling of analog and digital grounds. How the ground is arranged and where grounds are combined is often a crucial issue in board designs and often has a big impact on the performance of a system.

As well as being beneficial with design evaluations, the ECMC-Card also allows to conduct performance tests of the ADC and the LVDS chip. These performance tests are

[1] die: die means generally a silicon chip without the packaging around it

thought of as giving a realistic idea of what can be expected from using these chips in the final system.

6.2 Functional Description and Components

The ECMC is able to process two analog input signals. These get digitized to 12-bit precision by the two ADCs. As the Pre-Processor system only requires 10-bit precision, the two least significant bits are ignored. The two 10-bit wide words are then inputted into the LVDS transmitters. These are located at a distance of about 2 cm from the ADCs which is approximately the same distance from the ADC to the PPrAsic on the PPrMCM. This is done to obtain a realistic capacitive load of the signal tracks. The Phos4 chip allows one to adjust each clock phase of the two LVDS chips and ADCs individually. Figure 6.1 shows the functional block diagram. Inbetween the routing from the ADC to the LVDS

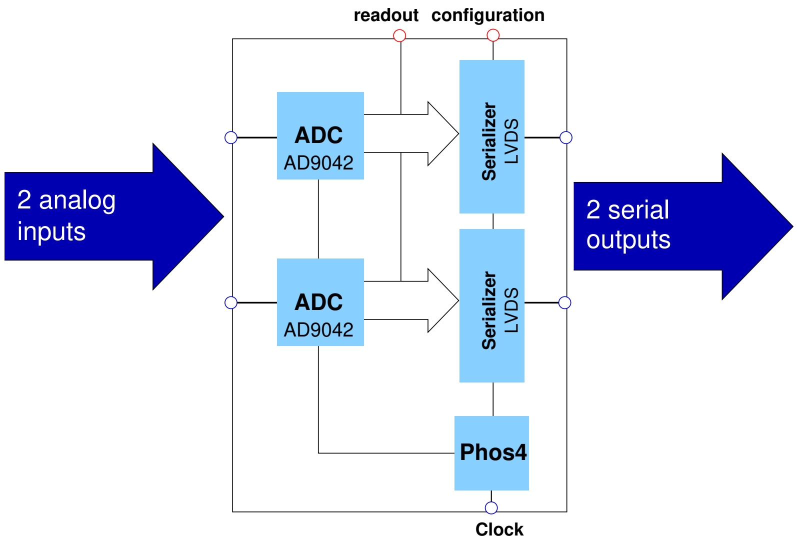


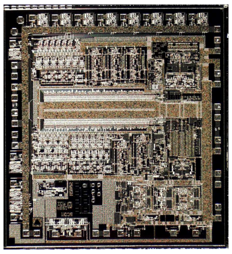
Figure 6.1: Functional block diagram of the ECMC-Card.

a 12-bit wide 'I/O bus' has been routed perpendicular to the buses which connect the two ADCs with the two LVDS chips. Combining these tracks with bonding wires or with soldered on cables allows one to read-out the ADC data directly or to provide data input to the LVDS transmitters. The LVDS transmitter provides a high-speed differential output of the serialized data coming from the ADC.

Two data channels have been chosen, where one ADC has output resistors and the other one does not. Other than that, the two channels are identical, thus allowing a direct comparison of the two.

The three different types of dies mounted on the ECMC will now be explained in more detail. There are two AD9042 analog-to-digital converters produced by Analog Devices [17], one Phos4 timer chip developed by the CERN-Microelectronics group [19] and produced by Austria Microsystems (AMS) and two LVDS serializers produced by National Semiconductor [20].

The AD9042 Analog-to-Digital Converter



The AD9042 is a high-speed monolithic 12-bit analog-to-digital converter. It is designed to operate at a sample rate of up to 40 MHz. So every 25 ns the analog input to the ADC is digitized and sent to the output. The AD9042 runs off a single +5 V supply voltage and provides CMOS-compatible digital outputs. This is useful, as it makes the layout of the MCM printed circuit board easier, as only positive supply voltages are necessary, +5 V and +3.3 V for the CMOS levels. The full range of the analog input is 1 Vp-p[2], which is centered at 2.4 V reference voltage, generated internally. The input range is therefore from 1.9 to 2.9 Volts. The most significant bit (MSB) of the digital output of the ADC is coded as twos complement. This results basically in an inverted bit. The consequence of this is that all bits change from low to high at an input signal which changes from 2047 to 2048, speaking in ADC code for a 12-bit[3] converter.

The architecture of the AD9042 is of a two-stage subrange type. Figure 6.2 shows a functional block diagram of this architecture. The analog input AIN drives an amplifier

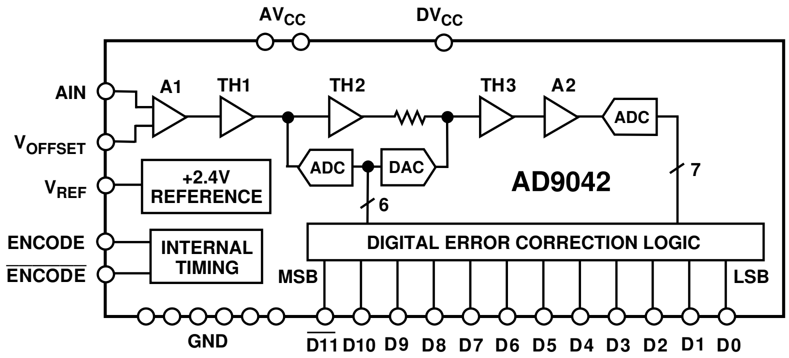


Figure 6.2: Functional block diagram of the AD9042 [17].

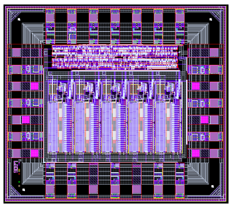
A1 where the reference voltage V_{REF} adds an offset to the signal. The output of A1 is held in TH1 at the logic high state of the applied clock (ENCODE). TH stands for track-and-hold, a module which can hold data for specific tasks. The held value of TH1 is then input to a 6-bit ADC, which does the first coarse digitizing. The digital output is then again transferred into an analog signal using a 6-bit digital-to-analog converter (DAC), which is accurate to 12-bits. At the input to TH3, the output of this 6-bit DAC is then subtracted from the delayed analog input signal which has been kept in TH2 to generate a residue signal. On a subsequent clock signal the residue signal is passed to TH3 and afterwards digitized by a 7-bit ADC. The 6-bit coarse ADC word and the 7-bit residue word are added together to form a 12-bit digital word. The one bit overlap between the coarse 6-bit ADC and the residue 7-bit ADC is used to correct for linearity errors. The total latency of the chip is 2.5 clock cycles, which corresponds to 62.5 ns. This is the

[2] p-p: the peak-to-peak value of the two maximas of an analog signal.
[3] 12-bit: $2^{12} = 4096$; therefore an ADC Code of 4096 is the maximum value.

duration of how long it takes until the digital data is valid at the output after having digitized an analog signal at the input.

The PPrMCM will only use 10-bits out of the 12-bits digital output to meet the required resolution of 10-bits as input to the PPrAsic. This is done by not connecting the two lowest bits. Measurement results on the AD9042 will be presented in Chapter 7.

The Phos4 Four Channel Delay ASIC



The Phos4 chip provides four calibrated delay lines for digital inputs. These can be programmed independently via an I2C interface, which is a serial interface needing only two control lines. The interface has been developed by Philips Semiconductors [25]. For each of the four input channels and the clock channel, a delay can be chosen between 0 and 25 ns in steps of 1 ns. The chip requires a 40 MHz reference clock as timing reference and runs from a 3.3 V supply voltage. Figure 6.3 shows the functional block diagram of the chip. The chip contains a delay locked loop (DLL) to provide the reference control voltage for the four delay channels.

On the PPrMCM, the Phos4 will be used to adjust the phase of the four ADCs. This enables the ADCs to digitize the analog input signal at its maximum value.

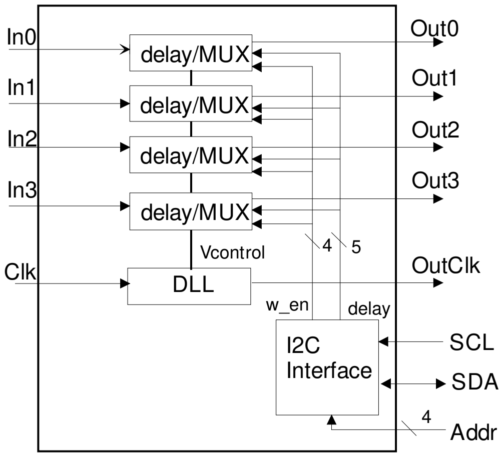
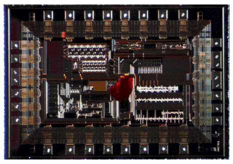


Figure 6.3: Functional block diagram of the Phos4 chip [19].

The DS92LV1021 Serializer



The DS92LV1021 transforms a 10-bit wide parallel CMOS data bus into a single high-speed LVDS serial data stream. It is designed to transmit data over differential backplanes or over Unshielded Twisted Pair (UTP) cable at clock speeds of up to 40 MHz. A start bit and a stop bit, added internally, frame the 10-bits of data. The start bit is always high and the stop bit always low. The serialized data and frame bits (10+2 bits) are transmitted from the serial data output at twelve times the applied clock. As the applied clock runs at 40 MHz, the serial data rate is $40 \times 12 = 480$ MBits/s. The two frame bits function as an embedded clock. Figure 6.4 shows a functional block diagram. In the Level-1 Calorimeter Trigger, serial LVDS links are used to transmit data from

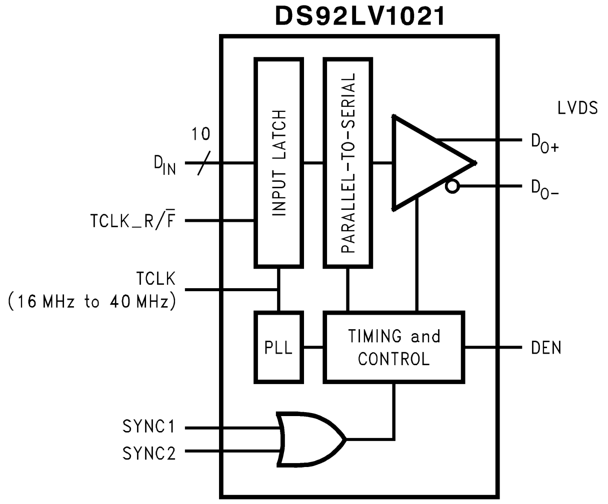


Figure 6.4: Functional block diagram of the DS92LV1021 [20].

the Pre-Processor to the subsequent Cluster Processor and Jet/Energy-Sum Processor. These processors use the corresponding receiver chips, the DS92LV1210, which perform the deserialization back from the high speed differential signal to a parallel 10-bit wide bus.

Before data can be transmitted, the deserializer PLL[4] must be synchronized to the Serializer. This is done by sending 'sync patterns' from the Serializer to the deserializer. This pattern, on which the deserializer can synchronize, is composed of six ones and six zeros switching at the input clock rate. A minimum of 1024 of such sync patterns need to be sent in order to 'lock' the link successfully and thus enabling the data to be transferred.

6.3 Design and Production Technique

The design of a printed circuit board (PCB) is done in three steps. First of all there is the schematic entry, followed by a physical layout, which is then converted into a file readable by the manufacturing apparatus. These steps have been performed using a software package provided by Cadence [34].

6.3.1 The Design Steps

The Schematic

The first task when building a PCB board is to create a schematic. Such a schematic consists of the logical wiring of signals and power lines between the used components. For

[4]PLL: Phase Locked Loop

this, libraries of the used components have to be created. The libraries contain layout information like pin count and pin name, as well as physical information such as power dissipation and package type.

The schematic entry tool Concept from the Cadence distribution has been used for this purpose. The obtained database is then forwarded to a tool where the physical layout can be entered.

The Physical Layout

Once the logical wiring in the schematic is done, the physical routing of wires and geographical placement of components has to be performed. This also requires libraries of the used components, now with detailed information on all layout dimensions. A library entry of a chip, for example, includes the dimensions of the chip area, the subjacent ground plane and the location and sizes of the bonding pads. Because there are no libraries for dies available from the manufacturer, effort has to be put towards their development. The Cadence tool Advanced Package Designer (APD) has been used for library creation as well as for layout routing.

MCM design constraints make it difficult to create the routing structures, as routing space is limited. For the ECMC, the fact that only two routing layers can be used (the top and bottom sides) adds another constraint whereas the MCM has four available layers. Nevertheless, the task was to obtain a realistic routing structure. Therefore, a signal line width of 150 μm and a line width for power and ground of 300 μm with a minimum pitch[5] of 100 μm have been chosen according to the values which are to be used for the PPrMCM.

Two different via sizes have been used to connect tracks on the top and bottom side of the PCB. A small one with a hole diameter of 300 μm and a thicker one with 800 μm in diameter. The size of the first one is limited by the size of the smallest usable drill and the latter has been included as the via can be easily assembled using through-hole track pins to provide the necessary connection.

The final step of the physical layout is to fill empty routing areas with ground planes for electric shielding purposes. For the ECMC, the bottom side is mainly used as a ground plane, but due to routing restrictions on the top layer, it also had to be used as a routing layer for a small number of signals.

Output Generation

After the layout is completed, APD generates a so-called ‘gerber file’ and ‘drill file’. These are ascii files which contain all the coordinates and dimensions of tracks, vias and ground planes needed by the manufacturing processes. As the ECMC has been produced on a circuit board plotter [35], these files need to be converted into a file adjusted to the requirements of the plotter.

[5] pitch:the minimal distance between two tracks

6.3.2 The Manufacturing Process

The circuit board plotter uses different sizes of cutters and drills to form the layer structure and the holes for vias. The smallest structures of 100 μm can be produced by the finest cutter. As this cutter has a very short life-time, the design has been optimized for a 200 μm spacing, using only a 100 μm for any necessary areas as well as for the footprints of the chips. Figure 6.5 shows the top layer after cutting and drilling by the circuit board plotter. Two parts should be distinguished. All the chips are located in an area labeled

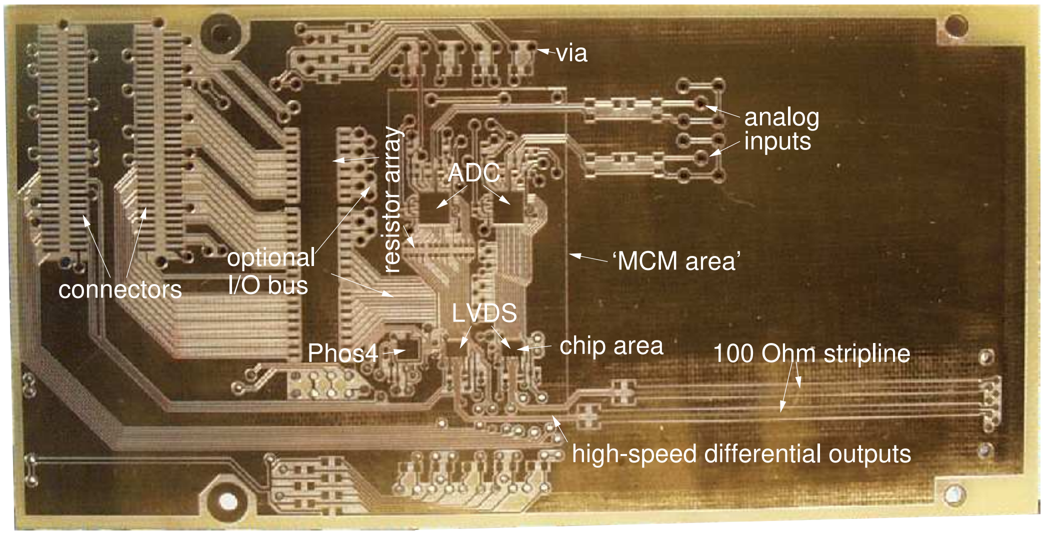


Figure 6.5: Top layer of the ECMC.

the 'MCM area', and the second section comprises of the rest of the board. For the 'MCM area', care has been taken to achieve a very realistic environment as on the MCM. It is for this reason that a line surrounds the 'MCM area', thus separating the ground plane physically from the board. The rest of the board hosts elements which will later be hosted on the PPM motherboard, such as additional block capacitors, resistors for the supply voltages and a filter for the analog inputs.

In Figure 6.5 one can also see the tracks of the optional I/O buses which end perpendicular to the data tracks connecting the ADC to the LVDS chip. At this point, a bond connection can be used to directly read ADC data out or to feed digital LVDS data in, but also to increase the capacitive load of the data tracks, which will be described in Chapter 7. All the control, power and ground tracks are routed to SMD connectors, where the left connector provides 3.3 V and the right one 5 V through the motherboard on which the ECMC-Card will be plugged on. The top side of the ECMC is gold plated for later bonding purposes, as bonding on copper does not work very well.

Microstriplines

For the high-speed differential outputs, a differential 100 Ohm microstripline has been designed to match the 100 Ohm twisted pair cable which transmits the data at 480 MBits/s. A mismatch in differential impedance between the microstripline and the cable would cause unwanted reflections. Figure 6.7 shows a schematic arrangement of a microstripline and defines the variables which influence the resulting impedance. Differential lines are

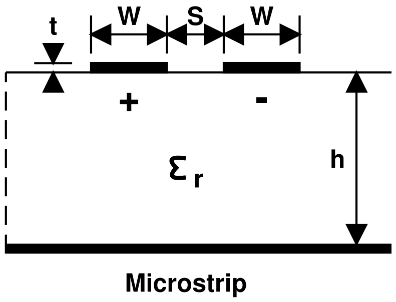


Figure 6.6: Arrangement of a microstripline [36].

used to confront the electromagnetic radiation caused by high-speed signals. Differential lines have equal but opposite signal levels. This means that concentric magnetic field lines tend to cancel and the electric fields tend to couple. These coupled electric fields are ‘tied up’ and cannot escape. Only the stray fringing fields are allowed to escape. This is a clear advantage to single-ended lines, where almost all the electric field lines are free to radiate away from the conductor.

To obtain the desired value of 100 Ohm, the line width w should be altered. The line spacing s should not be adjusted, as it should be the smallest spacing possible. For the ECMC, a minimal spacing of 100 μm has been taken. It is important to keep the spacing between the two differential lines to a minimum because the closer the two differential signals are, the tighter and better the coupling will be. This is illustrated in Figure 6.7. The formula to calculate the differential impedance Z_{DIFF}, has been taken from the ‘LVDS

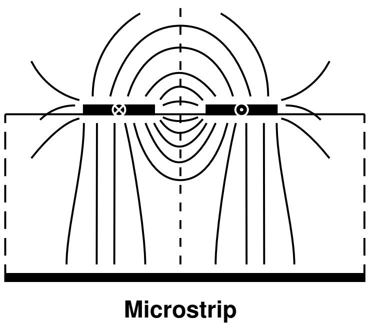


Figure 6.7: Ideal coupling of fields in a microstrip. [36].

Owner’s Manual’ provided by National Semiconductors [36]:

$$Z_{DIFF} = 2Z_0(1 - 0.48e^{-0.96\frac{s}{h}}) \text{ Ohm}$$
where
$$Z_0 = \frac{60}{\sqrt{0.475\epsilon_r + 0.67}} ln(\frac{4h}{0.67(0.8w+t)}) \text{ Ohm}$$

The variables are explained in Table 6.1. This formula has been plotted for the ECMC with the line width w as the variable. Figure 6.8 shows this dependency. This shows

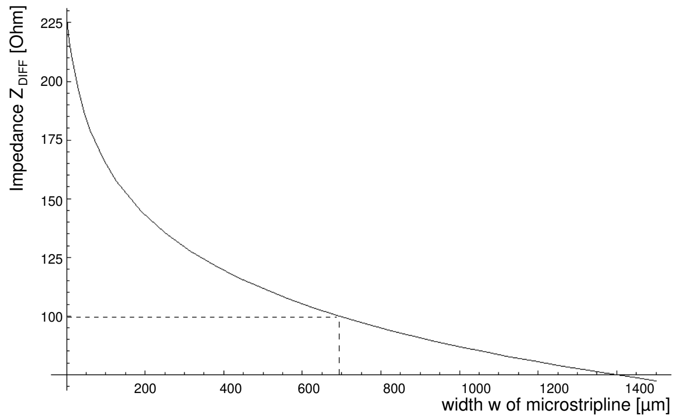


Figure 6.8: Differential impedance versus line width for the ECMC.

that for the ECMC, a line width of 680 μm results in a differential impedance of 100 Ohm. This formula has then also been applied to the layer properties of the PPrMCM. There a line width of 225 μm has been found to give a Z_{DIFF} of a 100 Ohm. This is also illustrated in Figure 6.9. The larger value for the ECMC is mainly due to the thicker layer of dielectric. The values for the PPrMCM come from the demonstrator MCM, see Figure 5.3, as the PPrMCM will be produced using the exact same layer structure as the demonstrator MCM. The PPrMCM with the four layers could also make use of striplines

	ECMC	**PPrMCM**
conductor thickness t	18 μm	25 μm
line spacing s	100 μm	100 μm
space between two layers h	1464 μm	190 μm
dielectric constant ϵ_r	5.4 (FR-4)	3.1 (Polyimide)
resulting line width w	680 μm	225 μm

Table 6.1: Used variables to obtain the line width for a 100 Ohm microstripline.

rather than microstriplines. Striplines use the same method as microstriplines, but are located in the middle of two layers. This is beneficial because it offers superior shielding between signals than the microstriplines. There are, however, some drawbacks, in that the signal suffers slower propagation velocity (about 40 % slower than microstrip) and additional vias are necessary, which cause reflections of the signals.

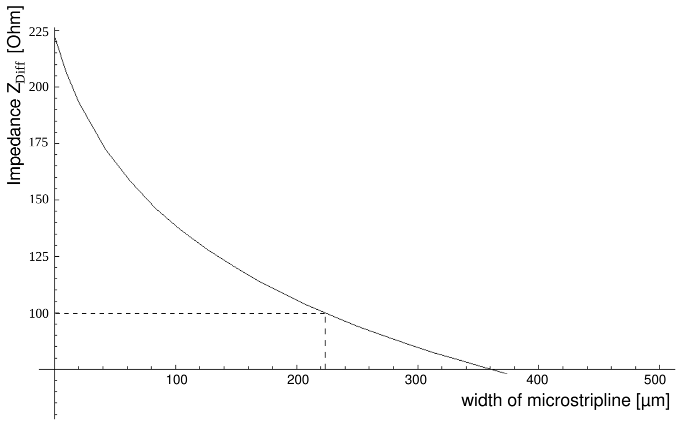
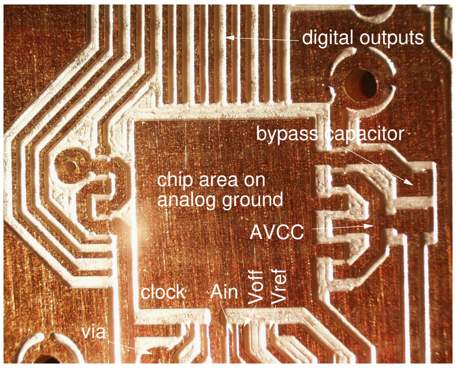


Figure 6.9: Differential impedance versus line width for the PPrMCM.

Footprints

The footprint of a die is the immediate surrounding of the die in terms of power and signal tracks, capacitors and resistors. For a die, all additional components that guarantee the proper functioning of the die (such as bypass capacitors and eventual resistors), and that are usually within the chip package, have to be provided.

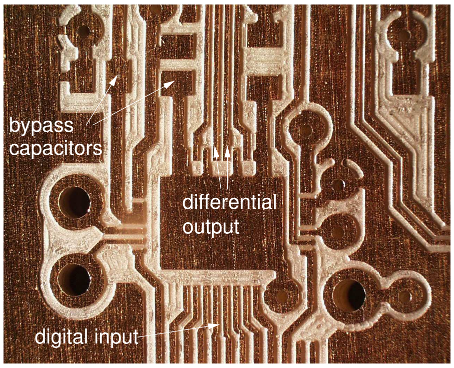


ADC Footprint

The picture on the left shows most of the footprint for the ADC on the ECMC. The chip area is connected to analog ground as the analog ground is expected to be 'calmer' than the digital ground due to the high frequency proportion in digital signals. The width of the signal tracks are 150 μm, the same size as the bondpads. Power tracks for supply voltage and ground are 300 μm. The 40 MHz clock signal to the ADC is routed on the bottom side of the ECMC and comes from the Phos4 timer chip. This has the advantage in that it has only a small influence on other important signals such as the analog input labeled *Ain*, which is located very close to the clock pad. The ADC internally generated reference voltage of 2.4 V can be used as offset voltage. This is done by tieing the pad for the reference voltage and the pad for the offset through a resistor. This cannot be seen on this picture.

Bypass capacitors are used to bypass the supply voltages. This is done separately for the analog (AVCC) and the digital (DVDD) supply voltages. This is necessary in order to maintain the integrity of the power distribution. The capacity between the supply pins of a chip and the corresponding ground counteracts the inductance of the finite length conductor which distributes the power to the circuits, providing a uniform supply voltage.

These bypass capacitors should be located as close to the power and ground pins as possible. As there will not be much extra space on the MCM, only one bypass capacitor of 100 nF is placed near the die. Additional capacitors are located on the motherboard.

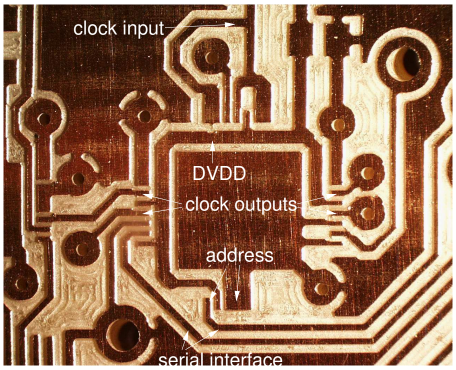


LVDS Footprint

In the case of the ECMC there is also one bypass capacitor near the die and two more, one with a capacity of 100 nF and the other with 2.2 μF further outside on the board.

In the picture of the LVDS footprint (see left), most of the track spacing is 100 μm. For example, the digital input bus track width is 150 μm with a 100 μm spacing inbetween. As the LVDS chip is not purely digital, it also has analog components like a PLL, the chip area is also connected to analog ground. As many as five control signals need to be introduced to the LVDS from the controller. This made extensive use of vias around the LVDS necessary in order to disentangle the signals into parallel buses.

Supply pads of the Phos4 chip are located on each side of the chip. Therefore, a supply ring around the ground area has been routed labeled 'DVDD' in the picture of the Phos4 footprint. As the Phos4 provides the clock, the ground area is connected to digital ground. The Phos4 chip is able to shift four different clocks separately. As in this application and also on the PPrMCM, only one input clock needs to be shifted for four dies. The four clock input pads and the actual clock for the Phos4 can all be combined. The Phos4 has to be addressed by a four bit word.



Phos4 Footprint

This address can be chosen individually and applied via the controller. On the ECMC the address has been chosen to be 8 and has been applied 'hard wired' by connecting the most significant address bit to the digital supply voltage and the lower three bits to ground.

Three of the output clocks are routed to the bottom layer immediately once on the board. For one of the two LVDS dies, this is not necessary, as the chip is located just next to the Phos4, getting its clock fed straight from the Phos4 on the top layer. The picture also shows the two signal lines of the I2C interface. The left is the serial data line and the right is the serial clock.

Assembly of the ECMC

For the assembly process, the same techniques have been used as was described in Chapter 5 for the demonstrator MCM. Only the mounting of the dies has been done prior to soldering. The reason for this is, that the ECMC does not have a soldering mask like the demonstrator MCM. The soldering mask prevents the flux from floating on the board and hence provides some security for the bond pads. Once they are covered by flux, bonding onto them is very difficult. Only those vias were soldered which would no longer be accessible once the dies were encapsulated. The following four pictures show the three different types of dies after being glued onto the substrate and bonding has been performed. A 25 μm aluminum bonding wire was used as was the case for the demostrator MCM. Figure 6.10 shows some views of the board after the dies have been mounted on. The first

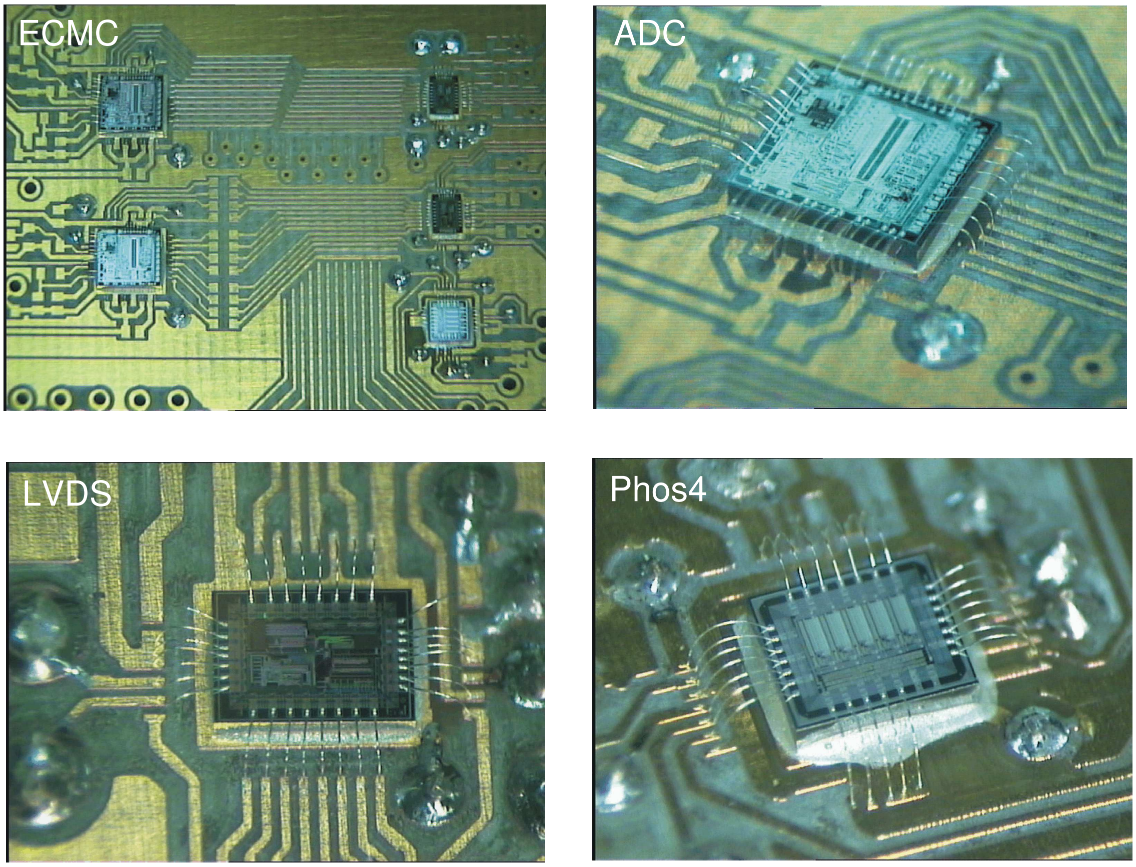


Figure 6.10: Three different types of dies on the ECMC.

picture in the top left shows an overall view of the five dies: The two ADCs on the left and the two LVDS chips and the Phos4 on the right. The following three pictures show the ADC, then on the bottom left side the LVDS chip and the Phos4 on the bottom right.

Power Tests

At this point the board is in a very fragile state. The chips have no protection and the wire bonds are easily damageable. Therefore, the chips need to be encapsulated. However, once they are encapsulated one is no longer able to exchange them if they are broken. For that reason, a power test was performed to all the chips. In this test, the supply voltages and the grounds have been applied using needle probes. The needles are put right on the power tracks which feed the chips. The current consumed by the chips is recorded and the obtained values can be compared with the chip's specification. If the values agree with the

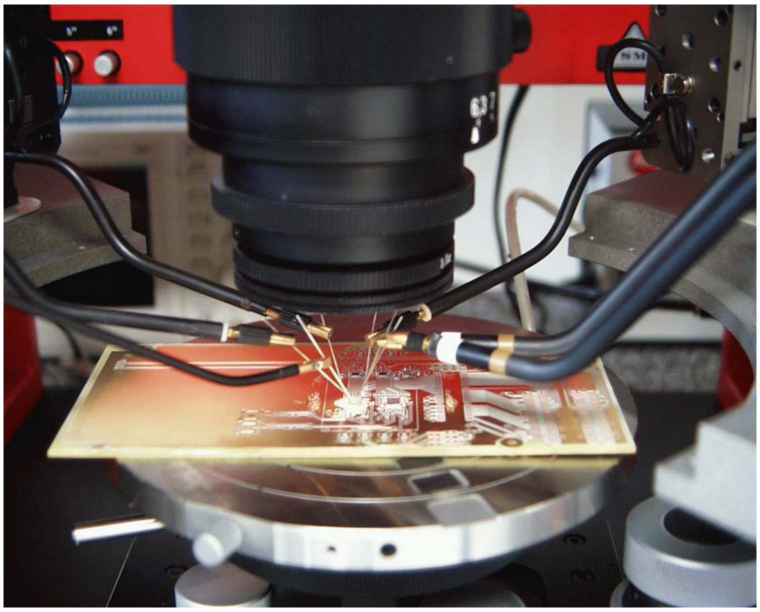


Figure 6.11: Set-up for power tests.

specification, the probability that the chip is working properly is increased. Figure 6.11 shows the set-up with the used needle probes. The power tests performed for the ECMC showed reasonable values. Table 6.2 lists the recorded currents and the values specified in the data sheet. The values for the ADC and the LVDS chip meet the values specified

supply voltage	**measured current**	**data sheet**
ADC: digital 3.3 V	8 mA	10 mA (5 V)
ADC: analog 5 V	110 mA	109 mA
LVDS: ana.&dig. 3.3 V	6.5 mA	4-10 mA
Phos4: digital 3.3 V	45 mA	$\geq$30 mA

Table 6.2: Recorded values for the power test.

in the corresponding data sheet. For the Phos4, the data sheet does not specify an exact value, as the chip can go into an undefined state before a reset or if no clock is applied.

After the power tests, the chips have been encapsulated using Glob-Top from Epoxy Technology Inc [37]. This is a thermally conductive two component epoxy. To prevent the Glob-Top from running over capacitor pads, which have not been yet equipped with a capacitor, a dam out of layers of adhesive tape was built around the dies. This simple method proved to work well.

6.4 Bringing the ECMC into Operation

Controlling the ECMC

Several control signals are required for the LVDS chips and the I2C interface of the Phos4 needs to be accessible. For these tasks an 'ECMC Controller' has been written in Verilog, a Hardware Description Language (HDL). The necessary logic was implemented in an FPGA[6] on the motherboard. This FPGA is an XC4010XL device from Xilinx [38]. The following tasks have to be performed by this controller:

- **Powering Up the LVDS Serializer**
  The LVDS chip must be powered up using a specific sequence to start it's PLL. If the sequence is not followed properly, the bus LVDS outputs might be stuck in a certain output state. This may occur if the clock input is driven before power is applied. The LVDS has a low active control signal called 'Powerdown'. If this signal is driven low, the PLL is shut down and the chip is put into a low power sleep mode. Cycling this Powerdown pin from high to low and back to high resets the PLL and returns the chip to normal operation. The proper sequence is to simultaneously power up the chip with the Powerdown pin held low for 1 μs. Once the supply voltage is stable the clock input can be driven.

- **Synchronizing the LVDS Serializer to the LVDS Deserializer**
  The Serializer has two control signals called Sync1 and Sync2. If one of the two signals are set high, the Serializer starts to send 'Sync patterns' on which the Deserializers PLL can lock to the Serializer. The Sync pattern consists of six ones and six zeros switching at the input clock rate. These Sync patterns should be asserted for at least 1024 cycles. When the Deserializer locks to the embedded clock of the bus LVDS the serial link is completed and the Deserializer output represents valid data.

- **Latching ADC data at the LVDS Serializer**
  The chip allows to select, if the rising or the falling strobe of the clock should latch the incoming data. A high of the corresponding control signal (CLK_R/F) selects rising edge, a low selects falling edge.

- **Controlling the I2C Interface of the Phos4**
  The different delays for the four clock channels in the Phos4 can be written into the chips delay-register over an I2C-bus interface. The I2C interface uses two signals SCL and SDA for data transfer. Eight bit words can be put on the SDA line which have to be followed by an acknowledge bit. Figure 6.12 shows a timing diagram of data transfer on the I2C-bus. For the Phos4, two 8-bit words are transmitted in one write cycle. The first 8-bit word specifies the address of the chip, for which the data is meant and the second 8-bit contains the value for the delay and the channel. The first three bits specify the channel and the following five the delay in ns. The delay can be chosen to be from 1 ns up to 25 ns in steps of 1 ns, or a static value of 1 or 0

[6]FPGA:Field Programmable Gate Array

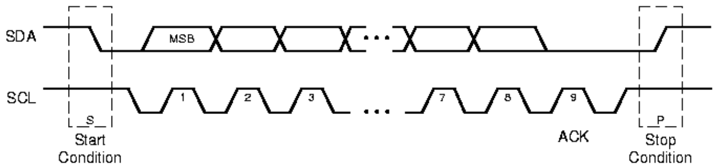


Figure 6.12: Data transfer on the I2C-bus [39].

can also be chosen for the individual clock outputs. For a detailed description of the data format see [19] and for a general I2C specification from Philips Semiconductors see [25].

Since the chip does not have a reset signal, it has to be generated from the I2C interface. The first negative transition on the I2C clock line is used to trigger the reset procedure. Therefore, the first data transmission will not have any effect on the delay registers.

The ECMC Controller is accessible through a VME-interface. Commands can be written to the interrupt register of a Dual Ported RAM from the VME side. Three types of commands exist. The command `Initialize` powers up the LVDS Serializer and synchronizes the LVDS Transmitter to the LVDS Receiver. The command `Set Phos4 delay` is accompanied with a 8-bit wide argument, consistent with the 8-bit data word for the I2C Interface, which contains the channel and delay information. The third command `Select Rising/Falling` also allows with an argument to directly set on which strobe the data in the LVDS device should be latched.

Timing Characteristics

For a proper functioning of the whole processing chain, it is important, that the data coming from the ADC is latched at the LVDS at a point where the data is stable. As the clock to the ADCs and the LVDS chips are all adjustable by the Phos4 such a point can always be reached. Figure 6.13 shows the timing between the ADC and the LVDS. The clock on the top is the 40 MHz clock provided by motherboard FPGA, which feeds the Phos4. The second clock is the first output from the Phos4 with zero delay, feeding the ADC. The data on the bottom is the least significant bit (LSB) from the ADC output which toggles. From this picture one can see:

1. As the Phos4 delay has been set to zero for the ADC clock output, the remaining 10 ns delay produced by the Phos4 are the internal routing chip delays (set-up time) t_s.

2. The output delay t_o of the ADC is about 9 ns. For the latency two clock cycles have to be added for the internal conversion time. The latency is the time between analog data is sampled and the time data is sent out of the chip.

3. A delay of 0 ns gives a stable timing configuration for all four clock outputs.

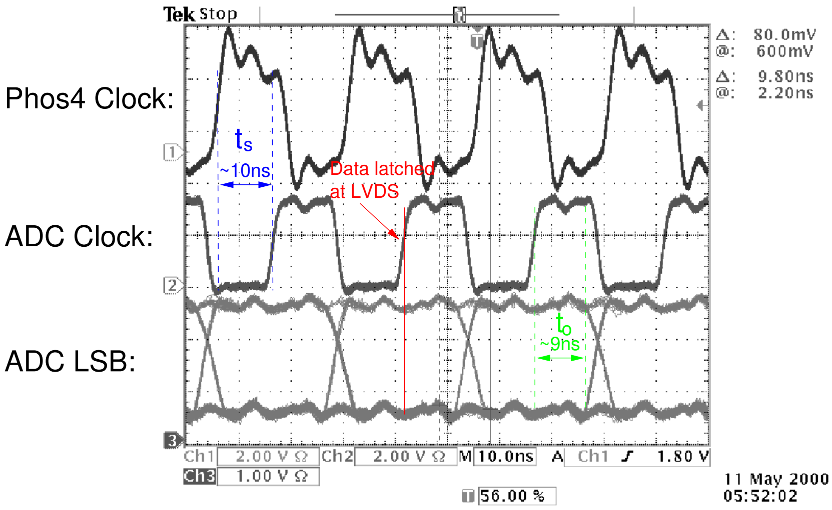


Figure 6.13: Timing between ADC and LVDS.

ADC Input

Because the ADC operates off a single +5 V supply voltage, the analog input needs an offset from ground by 2.4 V to center the input voltage range. The analog input is an operational amplifier configured in an inverting mode. 'Voffset' is the non-inverting input and is connected to the internal reference voltage of 2.4 V. Since the operational amplifier forces its input to the same voltage, the inverting input is also at 2.4 V. Therefore, the analog input has a thevenin of 250 Ohm in series with a 2.4 V source. Figure 6.14 shows a block diagram from this arrangement. For the use of the ADC on the PPrMCM, the

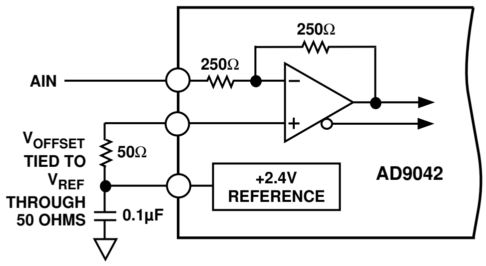


Figure 6.14: Offset adjustment with the internal 2.4 V reference voltage [17].

analog signal has to be DC coupled. A preferred AC coupling is not possible as an offset to the analog signal coming from the ATLAS Calorimetry needs to be added. This offset is independent from the offset used at the input and is used to 'DC balance' the analog signal. Since the input resistor of the ADC has a tolerance of 250 Ohm ±50 Ohm, this input stage is not straight forward and has to be designed with great care using active devices.

For the ECMC, an AC-coupling of the analog input has been applied, as a proper DC-coupling has not yet been designed. Figure 6.15 shows the AC-coupled analog input signal. The analog input is coupled with a 100 nF chip capacitor. R_T is the termination

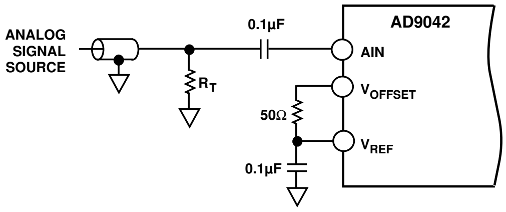


Figure 6.15: AC-coupled analog input signal [17].

resistor to match the 50 Ohm impedance of the coaxial cable.

Chapter 7

Measurements with the ECMC and Results

This chapter presents first measurements with the ECMC card and its results. For measurements concerning whether or not the ADC needs current limiting output resistors, the capacitive load on the output of the ADC on the ECMC card should have comparable capacitive load to the ADC on the PPrMCM. This chapter starts with an inspection of estimated capacitive loads for the ECMC and the PPrMCM.

Output Loading

The question, whether or not the ADC needs output resistors to limit its output current is an important design issue for the PPrMCM. As four ADCs are going to be mounted on one MCM and each ADC would have 10 output pins, a total of 40 output resistors would be needed. These would be arranged in SMD 0805 arrays of four resistors in one array. Ten arrays would therefore be needed, which would occupy approximately 20% of the total MCM area. This is clearly not desired due to limitation of space, and hence depends on the suitability of this ADC device at all.

Analog Devices support their suggestion to use output resistors in the data sheet of the AD9042 [17] with the following considerations: The AD9042 has a constant slew rate at the output stage of about 1 V/ns, which is independent of the output loading. A typical CMOS gate combined with a PCB trace and through hole will have a load of approximately 10 pF. Ten mA ($10pF \times \frac{1V}{1ns}$) of dynamic current per bit can therefore flow out of the chip. This then can cause, that up to 120 mA ($12-\text{bits} \times 10\text{mA/bit}$) of current can flow through the digital output stage.

As the PCB traces on the PPrMCM are going to be very short the capacitive load should be less than the mentioned 10 pF. A theoretical estimate can be calculated using the following formula:

$$C = C_{sidewall} + C_{plate} \approx \epsilon_0 \epsilon_r [\frac{2\pi}{ln(1+\frac{2d}{h}(1+\sqrt{(1+\frac{h}{d})}))} + \frac{c-h/2}{d}]$$

The first part of the sum corresponds to the sidewall capacity and the second one to the capacity of a plate capacitor [40]. Figure 7.1 illustrates the parameters used in the formula.

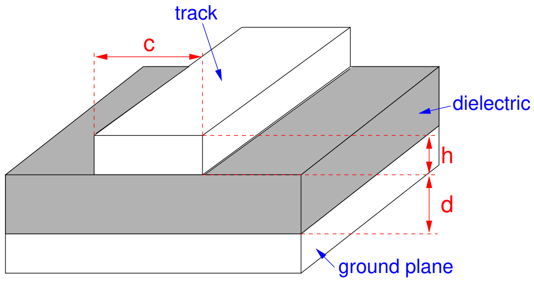


Figure 7.1: Schematic for calculation of capacitive load of a PCB track.

The capacitive load per mm has been calculated according to the previous formula for the ECMC and the PPrMCM. Table 7.1 lists the parameters and the results: According to

Parameter	**ECMC**	**PPrMCM**
track width c	150 μm	150 μm
track height h	18 μm	25 μm
dielectric width d	1464 μm	120 μm
dielectric const. ϵ_r	5.4	3.1
capacitive load/cm	0.55 pF	0.88 pF
capacitive load/2.5cm	1.38 pF	2.20 pF

Table 7.1: Used parameters for calculation of the capacitive load.

this formula, the capacitive load per cm on the MCM will be about 37% larger than on the ECMC. For the two ADCs on the MCM, the output tracks will be about 1 cm long, for the two further away from the PPrAsic, the tracks will be about 2.5 cm long. See Figure 8.2 for a first outline of the PPrMCM.

The pad used on the PPrAsic will have a similar capacitive load as the pad on the LVDS chip. This is typically about 1 pF. From that, one can expect a capacitive load of about 3.2 pF for the two ADCs further away from the PPrAsic, and about 1.9 pF for the ones closer to the PPrAsic.

As the track length on the ECMC is only about 2 cm long, the 'I/O bus', which has been described earlier, has been bonded on. This doubles the track length to 4 cm and gives a total capacitive load of about 3.2 pF including the LVDS pad - the same value as has been obtained for the PPrMCM.

This calculated value also agrees with a measurement which has been carried out using a differential probe. The probe was applied along a 10 Ohm output resistor, where a voltage drop of 30 mV was measured when the output made a logic transition from low to high. This corresponds to an output current of 3 mA or a capacitive load of 3 pF considering the slew rate of the ADC of 1 V/ns.

For a direct comparison of the performance, the ECMC uses one ADC with output resistors and one without.

7.0.1 The Measurement Set-up

The measurements have been carried out within the Pre-Processor test system environment. Two motherboards from the test system are needed for this set-up. The first motherboard carries the ECMC as a CMC daughtercard and the second one an LVDS receiver CMC daughtercard. Figure 7.2 shows a picture of the set-up. On the bottom picture one can see the fully assembled ECMC-card with Glob-Top encapsulation covering the dies. The processing chain will now be described. The analog input is fed into

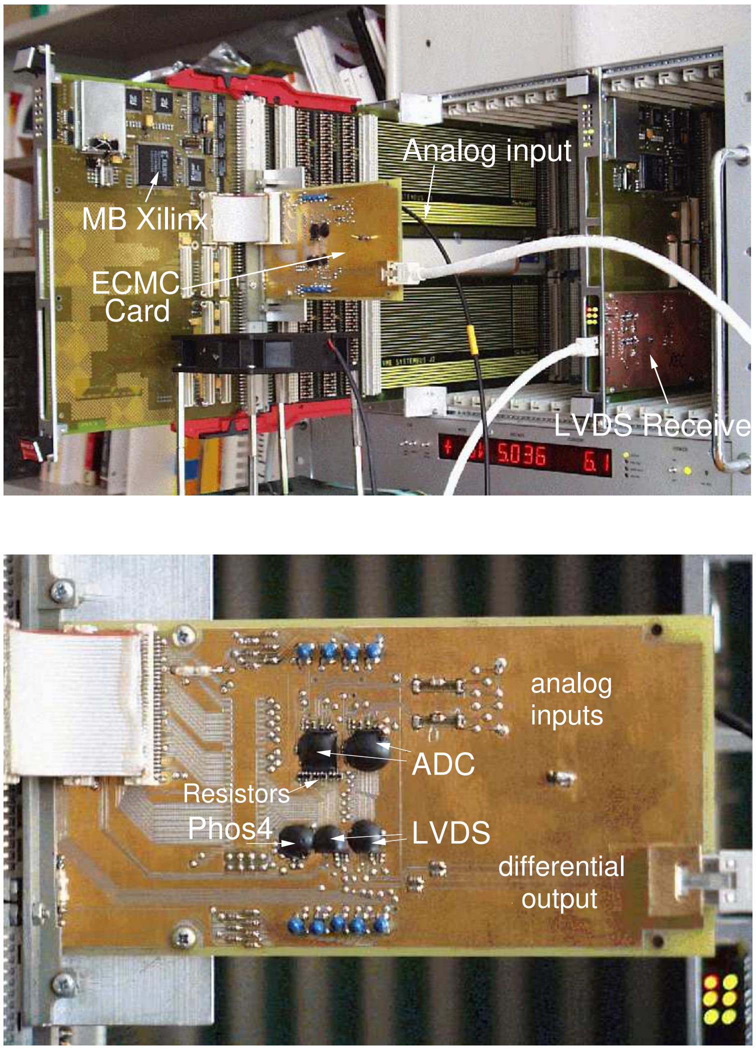


Figure 7.2: Test set-up within the Pre-Processor test system.

the ECMC via a coaxial lemo cable. After the signal has been digitized by the ADC, it is serialized to a 480 MBit/s differential signal and sent via a 1 m twisted pair cable to the LVDS receiver card on the second motherboard. This LVDS receiver decodes the serial bit-stream and provides the parallel output data to the motherboard FPGA. The FPGA latches the LVDS data from both LVDS-links (2×10-bit) and writes the data to the motherboard dual-port memory with a frequency of 40 MHz. A software routine reads the data from the dual-port memory. A server program running on the crate controller performs the actual hardware access. It decodes write commands and read commands, which were sent from the software routine client. Data packages are sent back via the TCP/IP network to the PC. There they are stored in a simple text format. Figure 7.3 shows the processing chain in a block diagram. As the ADC data is coded as twos comple-

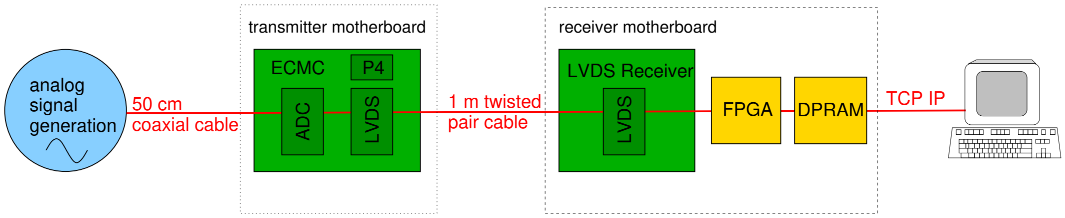


Figure 7.3: Processing chain of the test set-up.

ment, the most significant bit (MSB) needs to be inverted. This is done by the software routine which also converts the binary data into a decimal number.

7.0.2 The Task of the ADC and Locked Histogramming

A useful measurement should test the ADC within its planned application. The task for the ADC within the Level-1 Calorimeter Trigger is to digitize trigger tower signals coming from the ATLAS Calorimetry. Figure 7.4 shows a typical pulse coming from the liquid argon calorimetry which has been digitized. With the use of the Phos4, the ADC clock

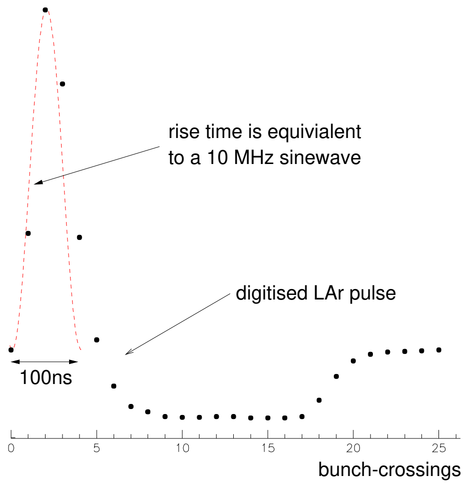


Figure 7.4: Digitized LAr pulse and 10 MHz sinewave fit.

will be adjusted so that the ADC takes a sample at the peak maximum. The peak of the pulse is the most important part of the signal because the digitized values on the peak are used for the BCID algorithm and the energy calibration. The undershoot is only used to 'DC balance' the signal.

In order to come to some sort of a conclusion as to whether or not the use of the output resistors makes a difference in the performance of the ADC, it would be good to have a measurement with statistics. As shown in Figure 7.4, the rising etch of the pulse can be approximated by a 10 MHz sinewave. If one uses a sinewave as the analog input, which is synchronous to the ADC clock, a statistical evaluation can be performed. The ADC will always digitize the sinewave input at the same position within its uncertainties. One is therefore able to look at the statistical distribution around the mean value. This measurement is referred to as 'locked histogramming' [41].

A synchronous sinewave to the ADC clock can be derived from the 40 MHz ADC clock itself. For this purpose, the ADC clock has been divided to a 10 MHz clock within the motherboard FPGA. This 10 MHz clock is then assigned to an output pin of the FPGA from where it can be applied to a filter in order to receive a sinewave. Figure 7.5 illustrates this procedure. The filter consists basically out of a 10 MHz quartz and two RC low-pass

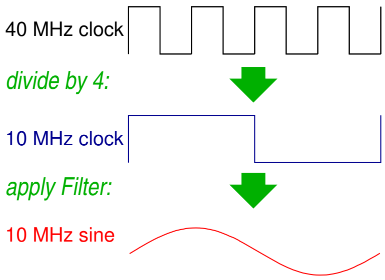


Figure 7.5: Process of how to obtain a synchronous 10 MHz sinewave.

filter in series. The use of a quartz has the advantage that little amplitude of the signal is lost. For a synchronous 10 MHz sine input, the ADC, running at 40 MHz, samples four values of one sinewave period. Figure 7.6 shows the derived sinewave as seen on the oscilloscope. In this picture, four sinewaves can be seen as the oscilloscope triggers on the

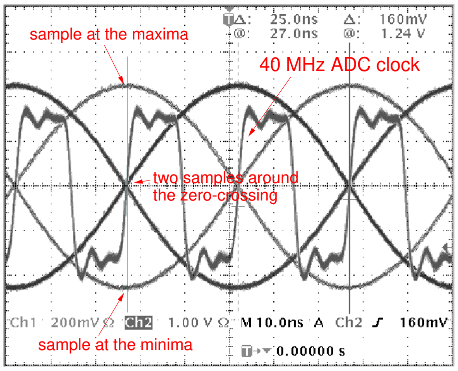


Figure 7.6: Picture from the oscilloscope showing the timing between the ADC clock and the sine input.

40 MHz clock. The timing between the ADC clock and the 10 MHz sine input has been adjusted, so that one sample is taken at the maxima of the sinewave, one at the minima

and two at the zero-crossings. This is coherent with the task of the ADC for digitizing an analog signal from the calorimetry, where the timing will also be adjusted in a way to take samples at the maximas and zero-crossings of the first part of the pulse.

For this locked histogramming measurement, a total of 819200 digitized values per ADC channel have been recorded. Since the dualport memory has a size of 8192 32-bit words, it had to be read out 100 times for each measurement run. This did not take much longer than a few seconds. The obtained data was then processed using the software tool PAW [42].

Figure 7.7 shows a histogram of the 819200 obtained values from a locked histogramming measurement. In this measurement, the 10 MHz sinewave had full-scale (1 Vp-p). The x-axis corresponds to the ADC code with 10-bit precision. A code of 1023 represents full scale. The y-axis, labeled 'number of occurrences' shows how often the same code occurred. The four peaks correspond to the four samples taken from the 10 MHz sine input

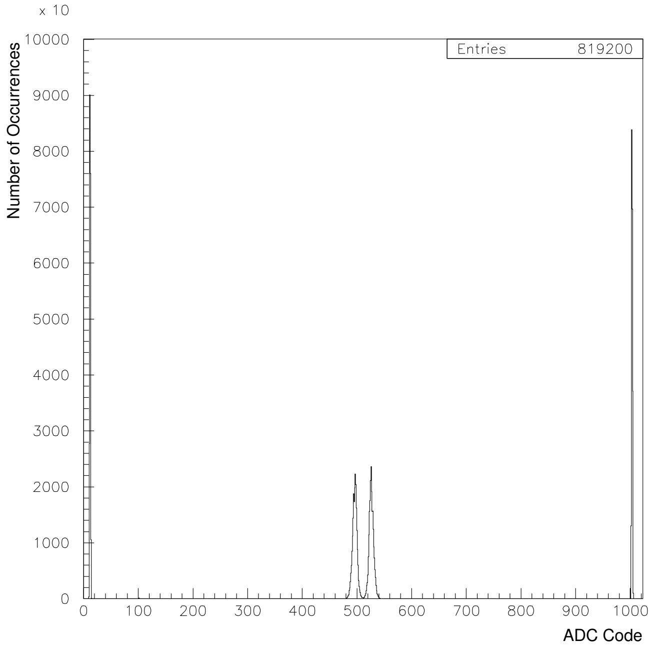


Figure 7.7: Locked histogram of a 10 MHz sine input signal.

by the ADC. Each of the peaks contains 204800 samples (819200 : 4). The difference in height is a result of the broader width of the samples taken at the zero-crossing. Figure 7.8 explains this behaviour. The same timing jitter, labeled 'Δt' in the drawing, results in a different variation of the digitized value. The sample precision is therefore dependent on the slew rate of the analog input signal. At the minima and maxima of the sinewave, where the slew rate is small or even flat, the digitizing can be more precisely compared to the zero-crossing with a high slew rate.

The two channels on the ECMC, the one with ADC output resistors and the one without them, have now been applied to the same 'locked' input signal. To conceive a quantity of performance, a Gaussian fit has been performed to the individual peaks to

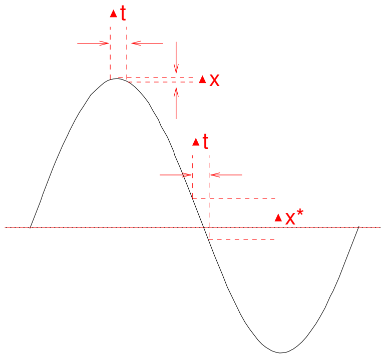


Figure 7.8: Influence of timing jitter on digitizing.

receive the standard deviation σ which then can be compared. Figure 7.9 compares the peaks from sampling at the maxima and at the zero-crossing. The two channels show a

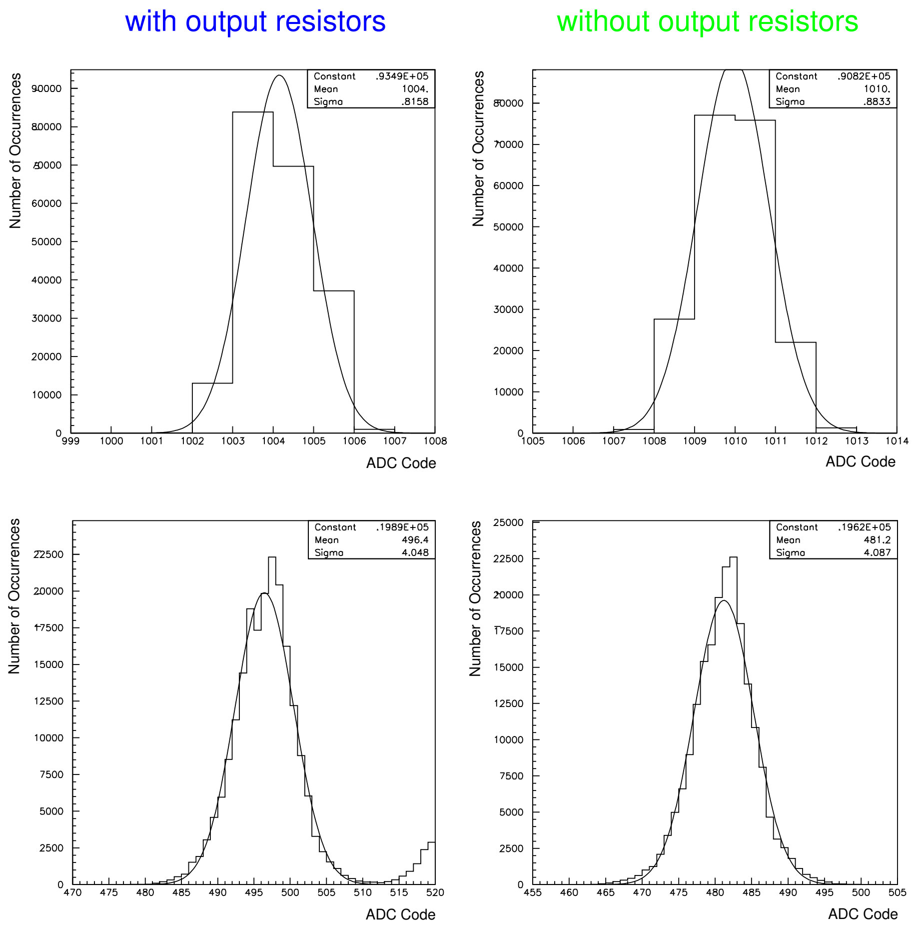


Figure 7.9: Peak from sampling at the maxima and zero-crossing for the two channels.

similar value for σ of about 0.8 for the deviation in sampling at the maxima, and σ=4 for sampling at the zero-crossing.

The reason why the two signals do not have the same mean, is due to the previously mentioned input resistor which has a broad tolerance. The analog input range for the two channels is therefore not exactly the same.

If one goes from a full-scale input to a smaller input voltage, the slew rate at the zero-crossing is also less steep, resulting in a smaller standard deviation. Figure 7.10 shows this for a half scale 10 MHz sine input. There σ is about 2 for the two channels. The relative

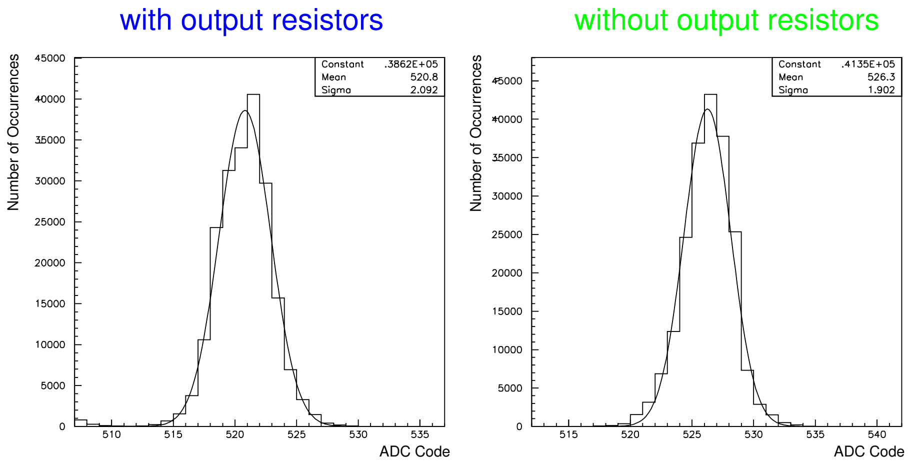


Figure 7.10: Peak from sampling at the zero-crossing of a 500 mV sinewave input for both channels.

uncertainly therefore remains unchanged.

An important outcome of these measurements is that no difference in the behaviour of the two channels has been found. The results also allows one to estimate what precision can be expected for the Pre-Processor system when digitizing an analog signal coming from the ATLAS Calorimetry.

7.0.3 Measured Performance of the ADC

The following measurements are mainly addressed to evaluate the performance of the ADC engaged under realistic condition with respect to the application in the Pre-Processor system. Nevertheless, these properties can also be used to compare the performance of the two channels in respect to the necessity of the output resistors.

For all measurements, a full scale sinewave from a function generator has been used as the analog signal source. There are two reasons for using a full scale sinewave as input signal. Signals which are less than full scale can produce misleading results as not all the possible ADC codes are tested. The second reason is, that ADC performance is generally slew rate limited. As already previously discussed, a full scale sinewave has twice the slew rate of a half scale sinewave at the same frequency. Performance for a half amplitude sinewave at a specific frequency cannot be compared to a full scale sinewave at the same frequency.

As only 10-bits of the ADC output are used the range in ADC code goes from 0 to 1023. The possible full scale input voltage is 1 Vp-p. Therefore, 1 LSB corresponds to about 1 mV.

Differential Non-Linearity (DNL)

Differential non-linearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. It can be written as:

$$\text{DNL} = V_{in}(Q_{i+1}) - V_{in}(Q_i) - 1\text{LSB} \tag{7.1}$$

where Q_i and Q_{i+1} are two adjacent quantization levels and $V_{in}(Q_i)$ is the analog input voltage which corresponds to the quantization level Q_i.

The measurement of the differential non-linearity has been carried out by using a sinewave from a function generator as the input signal. A frequency of about 10 MHz was chosen to test the ADC at an application specific frequency, as 10 MHz corresponds to the frequency of the rising edge of a typical analog signal from the liquid argon calorimetry. To prevent any statistical correlation, the ratio of waveform frequency to sample frequency should be irrational. As the sample frequency is 40 MHz, the sinewave frequency has been chosen to be 10.15 MHz.

Figure 7.11 shows the histogram for the two channels which is obtained by this measurement. The histogram shows the number of occurrences per ADC code. As is the case for the locked histogram a total number of 819200 samples have been recorded. The ADC

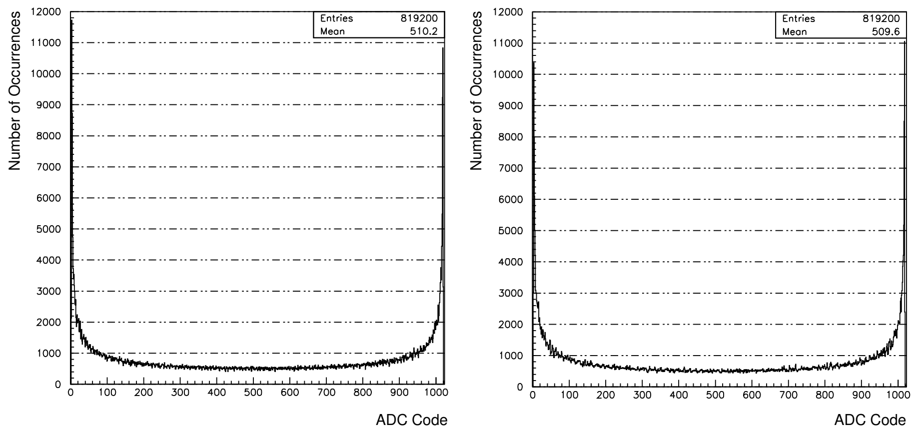


Figure 7.11: Histogram obtained for the two channels when sampling a 1Vp-p 10.15 MHz sinewave.

codes are unequally distributed and show larger occurrences at the two boarders than in the middle of the full scale range. This is due to the shape of the sinewave favoring high and low values to values in the middle range where the slope is large. A qualitative statement can however already be derived. Large differential non-linearities would show up as spikes and a missing code would have no occurrence.

For a quantitative evaluation however, the probability of occurrence of the different codes has to be considered in the calculations. The probability of occurrence of the i'th code P(I), is given by the following formula [41]:

$$P(I) = \frac{1}{\pi}(sin^{-1}[\frac{V(I-2^{N-1})}{A2^N}] - sin^{-1}[\frac{V[(I-1)-2^{N-1}]}{A2^N}]) \tag{7.2}$$

V is the full range of the ADC, A the peak amplitude of the input sinewave and N the number of ADC bits. The differential non-linearity is then computed from [41]:

$$\text{DNL} = \frac{\text{actual probability (i'th code)}}{\text{ideal probability (i'th code)}} - 1 = \frac{x_i/X}{P(I)} - 1 \tag{7.3}$$

where x_i is the number of counts in the $i'th\_code$ and X represents the total number of samples. Figure 7.12 shows the result for the two channels. For both channels, the peak

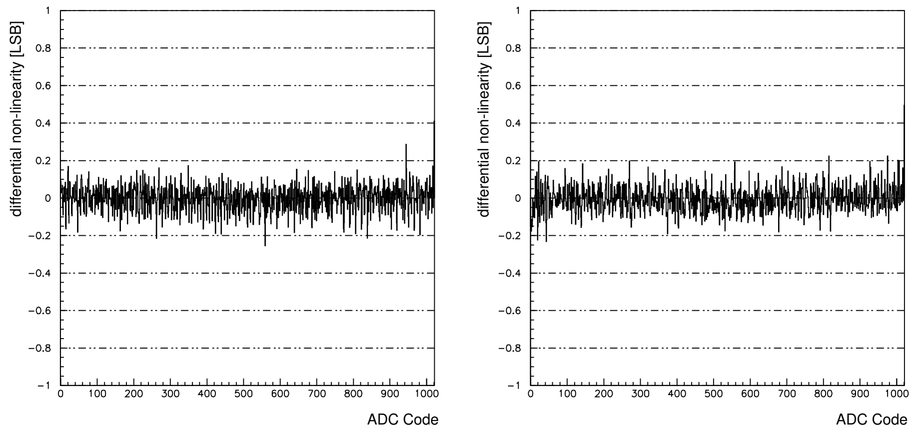


Figure 7.12: Differential non-linearity in LSB for the two channels.

values of differential non-linearity amount to ± 0.2 LSB for a sample rate of 40 MHz and a full scale sinewave input of 10.15 MHz.

Integral Non-Linearity (INL)

Integral non-linearity is the deviation of the ADC transfer function from a best fit straight line. Integral non-linearity does not include any gain and offset errors.

If the differential non-linearity is already known, the integral non-linearity can be calculated by summing the individual DNL errors up to the considered ADC code. Then a straight line is fitted to the resulting values. The integral non-linearity is obtained by correcting the calculated INL values to the offset and the slope of the fitted curve.

Figure 7.13 shows the integral non-linearity which correspond to the differential non-linearities in Figure 7.12. The peak integral non-linearity for both channel amounts to about ± 2 LSB.

Effective Number of Bits (ENOB's)

The effective number of bits is the measure of an analog-to-digital converters dynamic performance expressed in terms of number of bits. This number is related to the number

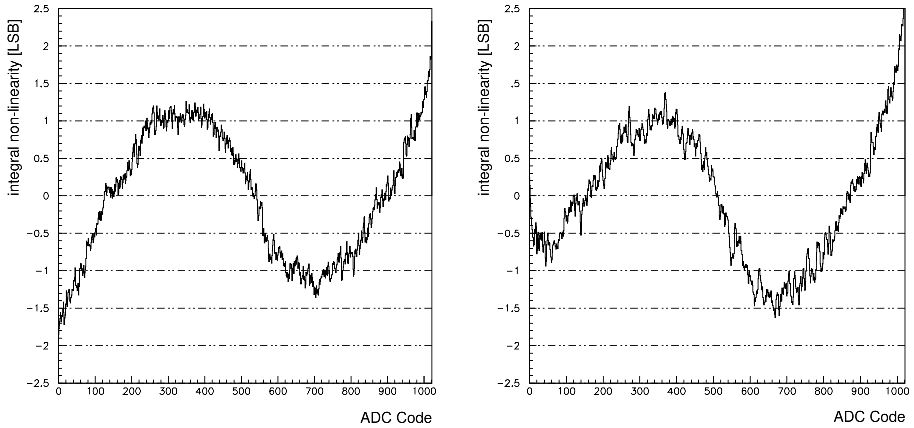


Figure 7.13: Integral non-linearity in LSB for the two channels.

of digital output bits but differs in that the digital output bits determine the theoretical performance while the effective number of bits represent the actual performance level of the converter.

No system is ideal. Every ADC has non-linearity, noise from reference voltages and aperture jitter. Every system adds noise to the analog signal being sampled and has some amount of clock jitter. All these elements contribute to system performance degradation with respect to the ideal system.

The effective number of bits can be determined by sampling a pure sinewave. This sinewave should cover the full range of the analog ADC input. A sinewave is then fitted to the acquired digital data and the RMS[1] value of the deviation between fitted and measured values is calculated. The obtained error represents a realistic value since it is measured under typical operating conditions therefore taking all effects influencing the ADC performance into account. Figure 7.14 shows the difference between measured and fitted values for a 3.6 MHz input signal. In the left graph it shows the deviation to the fitted sinewave for each code individually. The corresponding histogram is plotted next to it, showing how often certain deviations occurred. The equation for the effective number of bits is as follows:

$$\mathrm{ENOB} = n - log_2 \frac{\mathrm{RMS}_{\mathrm{true\ noise}}}{\mathrm{RMS}_{\mathrm{quant.\ noise}}} \tag{7.4}$$

The quantization noise occurs because an analog signal is sampled and its output code is represented by a finite number. Each sample has a quantization error of up to ± 0.5 of the LSB due to the difference of the true analog voltage and the code represented by the ADC output. The ideal error corresponding to the quantization noise is calculated by converting the fitted sinewave into digital values using a simulated, ideal ADC for which the RMS value of the deviation between fitted curve and simulated values is determined. The quantization error which has been obtained from a fit for a 3.6 MHz sinewave has been plotted in Figure 7.15. Applying the described method to different input signal frequencies for the two channels resulted in the effective number of bits graphs in Figure 7.16. The

[1]RMS:Route Mean Square

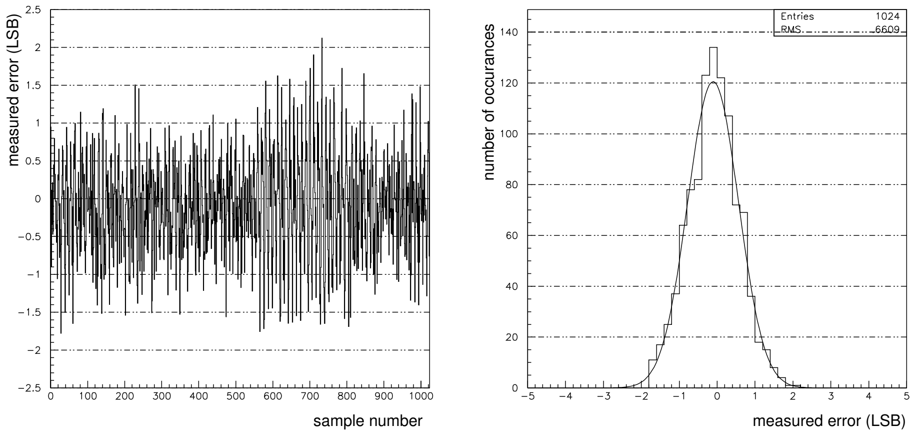


Figure 7.14: Measured ADC error: Error for each code on the left and the corresponding histogram on the right.

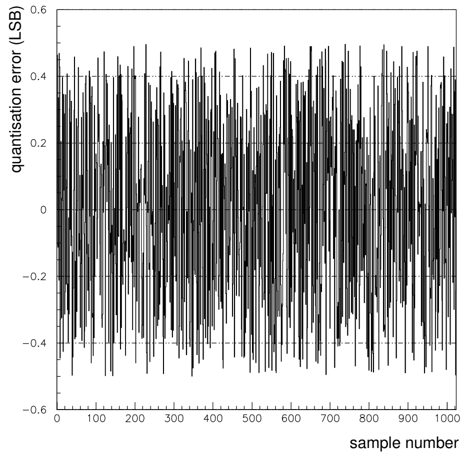


Figure 7.15: Ideal ADC error (quantization noise).

sample frequency was 40 MHz. The analog input signal has been filtered again by a quartz and a subsequent low-pass and high-pass filter. For both channels, a drop in ENOBs is observable. From an initial value of 8.9 at 1.8 MHz, only 7.8 effective bits are left at an input frequency of 9.9 MHz. The obtained values depend very much on the analog input signal, that is why a narrow filter is essential for the measurements. It has been observed that for the described test set-up, the effective number of bits dropped on average by one bit, when the filter was omitted.

Another conclusion can be derived concerning choosing a converter. For high-speed applications like this, one cannot expect to obtain a n-bit performance from a n-bit converter. This has been and still is subject of several articles [43]. For the Pre-Processor System, eight effective number of bits are sufficient, as only 8-bits from the raw 10-bit ADC data are kept after the energy calibration by the PPrAsic has been performed.

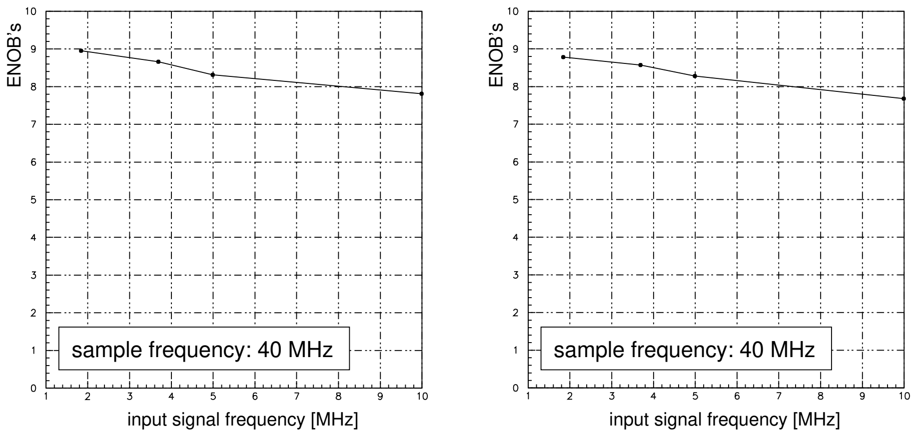


Figure 7.16: Effective number of bits for the two channels at different input signal frequencies.

Power and Ground Management

The method of determining the effective number of bits was also used to evaluate power and ground management on the ECMC. For this reason, 'optional vias' were included in the design of the ECMC. This vias connect, once they are equipped, supply voltages and grounds of the ADC.

Measurements have been performed on connecting the digital and analog grounds of the ADC and on connecting the digital supply voltages and the analog supply voltages of the two ADCs. None of the results differed from the measurement results performed with separated power and ground tracks.

Chapter 8

The Pre-Processor Multi-Chip Module

Multi-Chip Module technology often comprises a larger number of dies, each specialized for its specific task. It often combines mixed signal components with pure digital parts, made out of different semiconductive materials. These components are then all centralized in one encapsulated module. The motivation to use this technology for the Pre-Processor

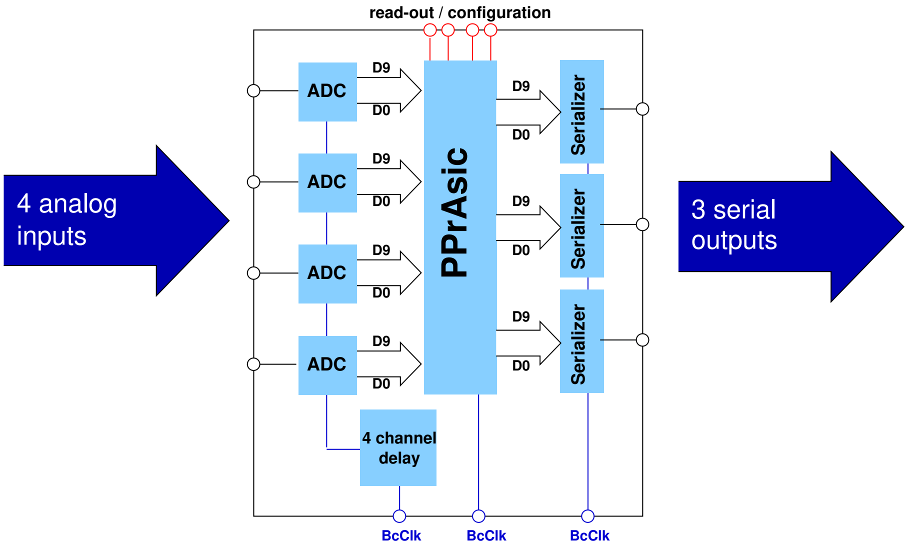


Figure 8.1: Block diagram of the Pre-Processor Multi-Chip Module.

of the ATLAS Level-1 Calorimeter Trigger comes mainly from two constraints:

- The first one is the latency consideration. The Pre-Processor is only allowed to use 18 bunch-crossings (450 ns) to process the incoming trigger towers and hence has to be very compact.
- The second reason is modularity. The Pre-Processor is located at a responsible position, as all data coming from the ATLAS Calorimetry has to be pre-processed.

Upcoming failures have to be easily repairable.

With the use of the PPrMCMs as the major component of the Pre-Processor system a compact system can be obtained which also allows to easily exchange faulty modules.

Figure 8.1 shows a coarse block diagram of the PPrMCM. From that figure, one can see, that only analog input and control signals go into the MCM package and only high speed serial data come out of the package. All digital buses are kept internal.

8.1 Layout of the PPrMCM

There are several issues which have to be considered for the layout of the PPrMCM. An important point is to keep analog parts away from digital parts as digital signals with a high frequency proportion in rising pulse edges can couple crosstalk into the analog signals. This applies especially to clock signals which have to be routed with great care. The individual chip supply voltages and ground signals should also be kept separate to avoid negative influence due to different behaviour.

Figure 8.2 shows an outline of the PPrMCM. The digital components and the analog

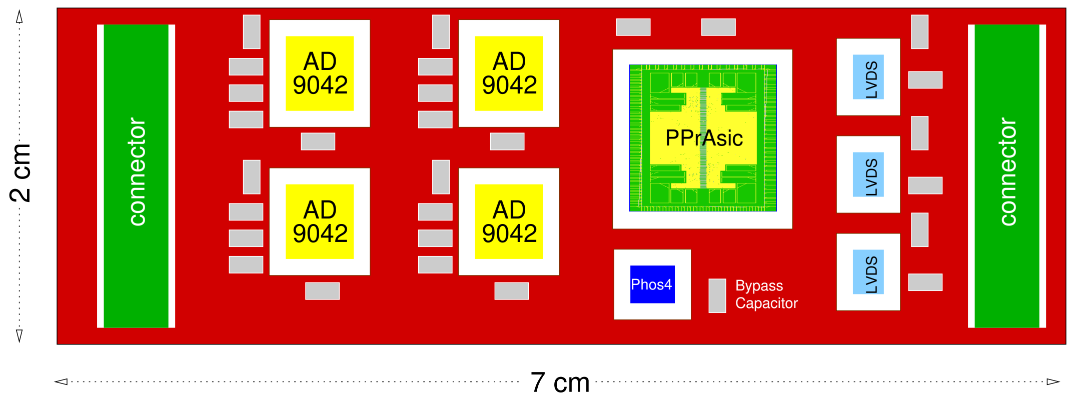


Figure 8.2: Pre-Processor Multi-Chip Module outline.

components are, as claimed, separated. The left side of the MCM with the four ADCs and the first connector contains analog parts whereas the right side, with the PPrAsic, the Phos4, the three LVDS chips and the right connector, is digital processing only.

The aspect ratio of 2×7 cm has been chosen to fit 16 MCMs on one Pre-Processor Module as shown in Figure 4.2, to obtain a system where 64 channels are processed on one PPM. For a uniform heat distribution, the distance between the components should be organized to an optimum, still allowing proper routing. The white rectangulars surrounding the chips symbolizes the area which will be occupied by the ground plane, where the chips will be glued on, and the substrate pads.

Table 8.1 lists interesting layout properties of the PPrMCM. For comparison, the corresponding properties of the demonstrator MCM have also been listed. Even so the total number of dies remained the same, the ratio of silicon-to-substrate area doubled. This does not cause a big problem, as the total power consumption dropped by more than

Layout Properties	PPrMCM	demonstrator MCM
Substrate dimension	2 cm×7 cm	3.7 cm×4.3 cm
Substrate area	14 cm^2	15.9 cm^2
Number of dies	9	9
Number of layers	4	4
Total power consumption	4.2 Watt	9 Watt
Number of wire bonds	390	470
Connector pin count	100	120
Number of capacitors	29	26
Silicon area	152.24 mm^2	80.15 mm^2
Ratio silicon/substrate area	10.9 %	5 %
Encapsulation	lid	Glob-Top

Table 8.1: PPrMCM and demonstrator MCM layout properties.

a factor of two. This is mainly due to the change from the high power consuming G-link serializers to low power LVDS devices.

Another change addresses the encapsulation. As the PPrMCM has to be in operation for over 10 years the used encapsulation is not allowed to corrupt the bonding wires due to aging process. As there are no reliable statistics available for Glob-Top by now, an aluminum lid covering the whole MCM is used instead. The inside will be filled with silicone gel to protect the dies from erosion and moisture.

8.2 Thermal Simulations

The thermal behaviour is always a critical issue in designing electronic systems, as the failure rate of electronic devices has an exponential dependency on the operating temperature. To evaluate the temperature distribution on a Pre-Processor Module caused by the 16 PPrMCM and to obtain a optimal arrangement of them, a thermal simulation has been performed.

To analyze the thermal characteristics of the PPM, the analysis tool DF/Thermax$^{\mathrm{TM}}$ [44] has been used. It is part of the Cadence product distribution [34] and is integrated in the Advanced Packaging Designer (APD). The algorithms implemented are based on an iterative numerical technique and allow thermal analysis by finite differences.

The DF/Thermax$^{\mathrm{TM}}$ simulator uses simplified information of the module build-up as input. It needs a simplified cross-section of used materials and the arrangement of adjacent layers, a description of the MCM attachment and information about the geometry. The necessary values for thermal resistance of the MCM junction to the top and bottom side and the thermal resistance of the MCM connectors where obtained as an outcome of a thermal simulation of the PPrMCM [45].

Hence, for the thermal simulation of the PPM, a MCM is seen as one device, plugged onto a 8-layered PPM via a 80 pin connector not resolving the individual chips. The total power dissipation of one MCM is about 4.2 Watt. This value is obtained by simply adding all the power consumption of the individual chips. Table 8.2 lists this calculation. The

Chip	**Power consumption**
ADC (AD9042)	4×595 mW
LVDS (DS92LV1021)	3×140 mW
Phos4	200 mW
PPrAsic	1200 mW
Total power consumption	4.2 Watt

Table 8.2: Total power consumption of the PPrMCM.

value of 1200 mW for the PPrAsic is just an estimate as the chip has not been produced yet. The estimation for assuming this value comes from the consideration that the FeAsic, the prototype of the PPrAsic, had a power consumption of about 300 mW. As the FeAsic was only processing one channel and the PPrAsic processes four channels in one chip the value of 1200 mW[1] was derived.

On top of that, the boundary conditions to the system must be defined. The edge guide resistances of the PPM printed circuit board (PCB) has to be specified. A resistance of 5°C/W in each direction has been applied. The initial temperature, the temperature of the board surrounding, and the fan air temperature were set to 25°C. The simulation also allows forced convection to be included. Fans blowing air with a velocity of 2 m/s over the top and bottom side where considered. This is a realistic value for fans used in VME crates. Table 8.3 summarizes the boundary conditions applied. Simulations for three

Boundary conditions	
PCB edge guide resistance	5°C/W
Constant temperature	25°C
Initial temperature	25°C
Forced convection	2 m/s
Radiation emissivity top	0.9
Radiation emissivity bottom	0.1
Distance to next PPM	2 cm

Table 8.3: Boundary conditions as applied.

different MCM arrangements on the Pre-Processor Module have been performed. Figure 8.3 shows the simulated temperature profile for the Pre-Processor Module PCB board. The configuration on the left, where the 16 MCM are just aligned on top of each other gives clearly the worst result in terms of high temperatures. The two other configurations show a similar maximal temperature of about 49°C, where the staggered configuration on the top left shows even smaller areas of high temperature. The disadvantage however for this configuration is, that the analog input signals for the eight MCMs on the bottom half

[1] recent simulation results from the PPrAsic showed a larger power consumption of 2.3 W

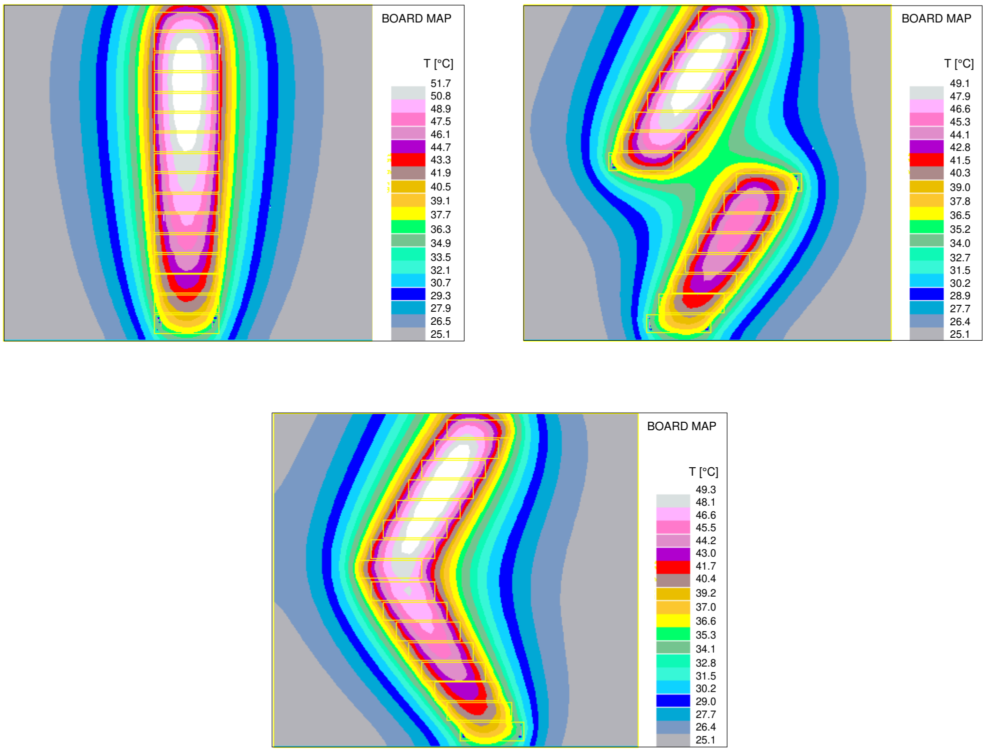


Figure 8.3: Temperature simulation for three different MCM arrangements: Board map.

have to pass the digital outputs of the ones on the upper half. A separation of analog and digital signals is also desired for the Pre-Processor Module.

The third configuration on the bottom fits very well into the overall architecture of the PPM board, which has been presented in Chapter 4 Figure 4.2. The maximal temperature on the board is 49.3 °C. The arrangement seems compact and balanced. Figure 8.4 shows the component map for the third configuration. The three colours for each MCM

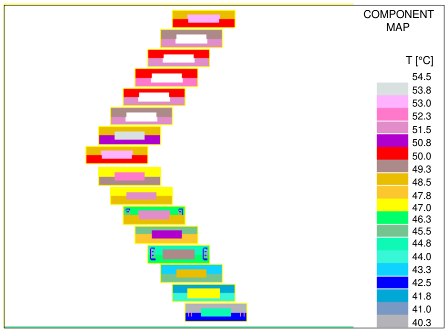


Figure 8.4: Temperature simulation: Component map.

represent the temperature on the top, at the junction and on the bottom of the MCM. The temperature ranges from 40.3 °C up to 54.5 °C. These values have to be seen as an average value. The individual dies on the MCM can be hotter [45].

The last simulation result shows the temperature distribution above the board. The fan blows air with a temperature of 25°C from the south to the north, or referring to Figure 8.5 from the bottom to the top. This agrees with the temperature profile in Figure

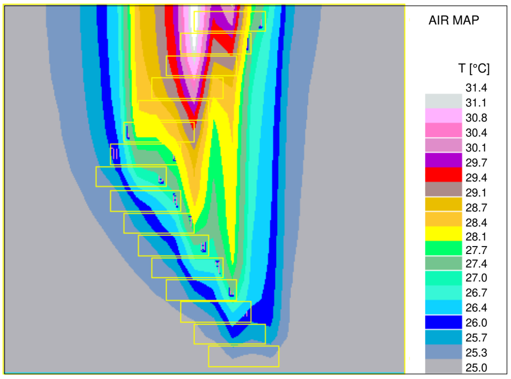


Figure 8.5: Temperature simulation: Air map.

8.5, where the air temperature on the bottom amounts to 25 °C and increases towards the top to a maximal value of 31.4 °C.

Summary and Outlook

This thesis described developments and investigations towards the building of a Multi-Chip Module for the ATLAS Level-1 Calorimeter Trigger. Six demonstrator MCMs have been assembled for the Pre-Processor Modular Test System. The experience gained will contribute to the assembly of the final Pre-Processor Multi-Chip Module.

There have been technological changes made to the demonstrator MCM in order to proceed to the making of the final Pre-Processor Multi-Chip Module. These changes include the increase in digitization precision from 8-bits to 10-bits and a change from G-link serializers to LVDS serializers. To investigate the interplay of these new components and to determine layout properties, an evaluation CMC card, called the ECMC has been successfully designed, manufactured and brought into operation. The ECMC card hosts three of the four types of the chips on the final PPrMCM, only the PPrAsic is missing. An ECMC controller has been written in Verilog, a Hardware Description Language (HDL), in order to access and control the chips.

The interplay between the chips has been proven to work and a footprint for each chip has been designed. Within the Modular Test System of the Pre-Processor, a test set-up with the ECMC was obtained, where an analog input signal is digitized and then serialized to a high-speed serial data rate of 480 MBits/s. The signal is then transmitted via a twisted pair cable to a deserializer receiver card, from where the digital output can be read-out by a PC.

This set-up was used to perform measurements to answer the question of whether or not the ADC needs current limiting output resistors. A comparison made of the performance of two channels, one with output resistors and one without, did not indicate any different behaviour between the two. This result allows one to use the chosen ADC on the Pre-Processor Multi-Chip Module. Output resistors would have occupied about 20% of the space on the MCM.

Performance measurements for the ADC with a constant sampling frequency of 40 MHz were carried out using the full test set-up as described above. The results of the performance parameters will now be discussed. A differential non-linearity (DNL) which is less than 0.2 LSB has been measured for an input signal of a 10.15 MHz sinewave. From this result, an integral non-linearity (INL) of about ± 2 LSB has been calculated. The effective number of bits (ENOBs) at an input frequency of 1.8 MHz is 8.9, which decreases to 7.8 for a 9.9 MHz sinewave.

Heat simulations were carried out for three different arrangements of the 16 PPrMCMs on a Pre-Processor Module. An arrangement in 'v-form' showed acceptable results with a maximal board temperature of 49.3°C.

In the near future, the ECMC card can be used as a data sink for the design of the analog line receivers which will be located on the Pre-Processor Module. It can also be used to investigate heat dependency on the high-speed LVDS-links.

With the results of the ECMC card, the design of the PPrMCM can now be completed. The manufacturing of the first Pre-Processor Multi-Chip Modules will start at the end of this year.

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Figure 8.6: The Heidelberg ATLAS group. From left to right: Myself, Prof. Eike-Erik Kluge, Volker Schatz, Ralf Achenbach, Bernd Stelzer, Dan Husmann, Klaus Schmitt, Cornelius Schumacher, Dr. Paul Hanke, Dr. Ullrich Pfeiffer, Michael Keller, Prof. Karlheinz Meier.