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Readout-Circuits for Superconducting Nanowire Single Photon Detectors

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Abstract

Superconducting Nanowire Single Photon Detectors (SNSPDs) provide high detection efficiencies and fast count rates over a broad wavelength range, leading to their use in many high performance applications. Due to their operation at cryogenic temperatures, readout via electrical wires is limited in scalability due to the wires' thermal load. An alternative interfacing strategy is provided by optical readout, which could offer lower thermal load and higher data transfer bandwidths via optical fiber interconnects.

To this end, I investigate in this thesis new possibilities of interfacing SNSPDs with electro-optic-modulators such that the SNSPDs voltage signals could be registered via optical readout. I propose and investigate three new interfacing circuits, which give rise to output voltages two orders of magnitude larger than reported for similar previous circuits, reaching the required voltage threshold for optical readout.

As a second part of this thesis, I set up a basis to conduct cryogenic heat transport simulations and present an interfacing circuit that incorporates a self-regulated electro-thermal switch. Finally, I fabricate and measure integrated chips to extract resistances of cryogenic thin-film resistors and critical currents of thin-film superconducting devices.

Contents

Chapter 1

Introduction

1.1 Motivation for this thesis

Detecting weak optical signals is of importance in a multitude of fields, e.g. communication [1], sensing [2], attempts at quantum computing [3] and fundamental physics [4]. Some examples include medical flourescence imaging [5], metrology of fundamental quantum states [6], deep-UV astronomy [7] and space communication [8].

To this end, Superconducting Nanowire Single Photon Detectors (SNSPDs) are a class of photodetectors that are able to detect light down to the single-photon level upon local suppression of the superconducting state due to photon absorption. This high sensitivity to single photons makes SNSPD especially usefull for applications where high detection performance is required [9].

A growing field of research is integrated photonics [10], where light is guided and manipulated within single chips. Fabrication of such photonic chips is done via litographic methods starting with initial wafers, which offer excellent spatial resolution down to the nm-level and high reproducibility.

SNSPDs can be integrated in such a photonic chips, tayloring their performance towards e.g. high count rates [11], low dark-counts [12], low jitter [13] and high detection efficiencies at broad wavelengths [14]. Compared to semiconductor-based photodetection, SNSPDs are especially competitive in the infrared (IR) and ultraviolet (UV) regimes [15].

The high integration density of SNSPDs motivates research also in the design of large detector-arrays, where thousands of detectors are integrated on a single chip in array-like fashion. Further scaling could allow such arrays of detectors to be used as cameras, especially for the UV and IR, with promising recent proof-of-concept demonstrations [16].

SNSPDs need to be operated at cryogenic temperatures in the range of 1-4K, requiring cryogenic systems. Each wire that is connected to such a cryogenic device introduces a thermal load. This limits the achievable number of simultaneously addressable devices to and from such a chip due to the limited cryogenic cooling power [17].

To improve on this limitation in multi-device addressability, research has been growing in the study of optical readout[18]. Hereby, on-chip electro-optic modulators (EOMs) link

electrical to optical signals, allowing to interface a cryogenic chip optically instead of with wires [19].

Using optical fibers to carry information from the cryogenic to the room-temperature world could allow for lower thermal load and higher data throughput, leveraging techniques such as wavelength division multiplexing [20]. This would be especially useful for densely-integrated chips. In aforementioned large-detector arrays, optical fibers could allow to address multiple detectors at the same time, which currently with electrical wires is not possible [21].

Optical readout of SNSPDs is a rather recent field of research, with first experimental demonstration by Cea et al. in 2020 [22]. In their setup, the detection was limited to UV photons and the the maximum photon count rate (on the order of 1MHz) was mainly limited by the reset time of the EOM.

1.2 This thesis work

In this thesis, I investigate whether optical readout of SNSPDs can be extended into the IR-sensitive regime and whether interfacing them with a different EOM design can result in shorter reset times.

To this end, I designed and analysed three new superconducting circuits that could interface a waveguide-integrated IR-sensitive SNSPD with an integrated-photonics-based $LiNb_3$-EOM, such that the generated optical modulation would be strong enough for optical readout.

These three interfacing circuits are reported in Chapter 3 and constitute the main work of this thesis.

In one of these circuit a thermal switch was included. Simulating its thermal properties at cryogenic temperatures grew into it's own Chapter, Chapter 2.

Finally in Chapter 4, I show three fabricated chips and characterize them, to test the performance of the proposed circuit components.

Chapter 2

Background

This first chapter is intended to give background knowledge to all the topics that are of relevance for this thesis. I first introduce SNSPDs and will then discuss strategies how their detection signal can be amplified and read out.

2.1 Superconducting Nanowire Single Photon Detectors

Superconducting Nanowire Single Photon Detectors (SNSPDs) are a specific class of photodetectors with allow to detect single photons. I introduce here first their general properties, their history, and the detection mechanism. Then I introduce four fundamental properties of an SNSPD. With these, one can describe it's most basic equivalent electrical model. I finish by showing a basic interfacing circuit and discuss the detection cycle and some resulting basic requirements on the circuit design.

2.1.1 Basics

SNSPDs are thin nanowires, ca. 100nm wide and ca. 5nm thick, which are made out of some superconducting material. In the top-down fabrication approach, the superconducting material is first deposited as a thin film on a wafer and then etched after lithography [9]. For integrated photonics, SNSPDs are patterned in a U-shape on top of a waveguide material. An impression of such an SNSPD is given in figure **??**, which displays the true relative sizes between width and length, as used for fabrication.

A typical superconducting material of choice is NbN [23][24], which has a relatively high critical temperature T_c of 8-10K and is polycrystalline. It proved to have good compatibility and yield with SiN, and due to it's faster thermal relaxation time it results in superior count rates compared to other materials such as NbTiN or amorphous silicides [25].

Silicides, such as WSi and MoSi, have the advantage of being amorphous, making them compatible with multiple platforms [26] [27]. They need to be operated however at lower temperatures, requiring sub-K cryogenic systems.

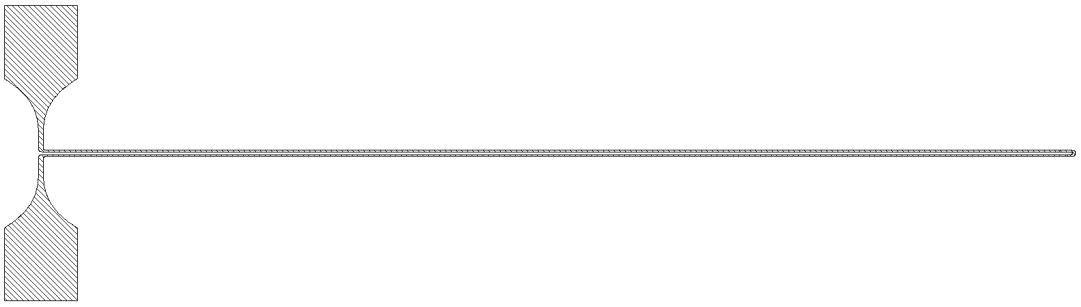

Figure 2.1: Design of an SNSPD at correct relative scale. The thin U-shaped part is sensible to photons, the large pads allow connection to electronic circuits.

Their amorphous structure results in slower thermal relaxation and thus reduced timing performances [28]. It has been observed that they can give a higher yield at large scales, which is why they can be a preferred material e.g. for large detector-arrays [16].

An SNSPD is operated as single-photo-detector by biasing it near to it's critical current I_c, which is the maximum current the SNSPD can support without breaking the superconducting state. When a photon impinges on the SNSPD and is absorbed, a local resistive domain forms across the nanowire, giving rise to a measurable voltage signal.

2.1.2 Integration on-chip

Two distinct geometries have emerged for how SNSPDs are patterned on-chip: Bulk-SNSPDs and waveguide-integrated SNSPDs [29]. The geometry is intimately linked to how light is coupled to each respective detector type.

Bulk SNSPDs are created by patterning the nanowire in a long meandering shape, such that it completely fills a specific area on the chip, typically on the order of hundreds of square µm's [30]. Light is coupled to such a bulk SNSPD via a lensed fiber that is placed vertically on top of the chip and collimates the light onto the meander area.

Waveguide-integrated SNSPDs are created by patterning the nanowire in a U-shape atop a photonic waveguide, with a typical length of 50-100 µm depending on the waveguide material and figure of merit for the specific detector [9]. This allows the nanowire to have a high detection efficiency, as the light for detection is guided directly below it. Waveguide-integrated SNSPD can achieve near unit detection-efficiency even in the low photon energy IR regime, as for example for the 1550nm telecom wavelength [31] [32] [33]. The ability to interface with the waveguides allows photon creation, manipulation, and detection all on the same chip [34]. The reduced footprint compared to bulk allows higher integration densities.

The material stackup of a photonic chip wafer is shown in figure 2.2. The upmost layer

is the thin film of superconducting NbN (5nm), from which the SNSPDs are patterned. The next layer is LiNbO3 (330nm), from which the integrated waveguides and electro-optic modulators can be fabricated [35]. The SiO (3.3µm) provides adhesion for the LiNbO-layer as well as a refractive index contrast, such that light guided in the LiNbO-layer does not leak into the substrate below. The Si (525µm) provides mechanical stability for the whole chip, i.e. it prevents breaking and bending.

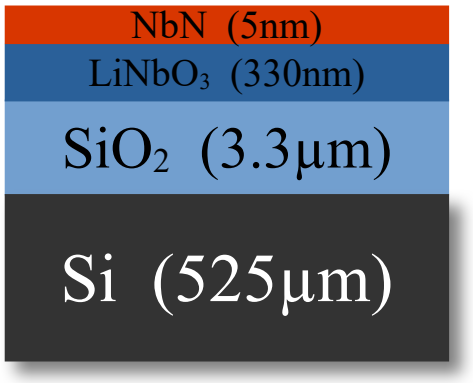

Figure 2.2: The wafer stack of a photonic chip. Waveguides and EOM are patterned into the 330nm $LiNbO_3$ layer, the SNSPDs into the 5nm NbN film. The SiO_2 provides refractive index contrast and the Si provides structural stability.

2.1.3 History

SNSPDs were introduced by Golt'smann et al. in 2001 [36], employing for the first time NbN nanowires for single-photon-detection, setting the basis for todays SNSPDs. Theoretical work in 2009 showed how such SNSPDs could be applied to integrated photonics [37], with first experimental realisations following by Sprengers et al. in 2011 [38] and and Pernice et al. in 2012 [29].

Before the advent of SNSPDs, superconductivity was already exploited for photon detection via other techniques. One of the most popular methods was (and is) the Transition-Edge Sensor (TES) [39]. Research into Transition-Edge-Sensors already started in the 1940s [40] and was refined from there on for decades [41] till today [42]. It is this long research into superconductivity, photo-detection, cryogenics and readout techniques from which SNSPDs could emerge. TES are employed in many areas of research, for example as large detector arrays in astronomy [43]. Their sensitivity and operation principle gives direct ability for photon number resolution [44].

TES can also serve as an instructive comparison to appreciate how SNSPDs differ from their predecessors. TES are operated in the superconductivity transition range very close to T_c, while SNSPDs are operated well below T_c. In TES, an absorbed photon modifies the resistance of the detector by locally increasing the detectors temperature. To be this sensitive, TES need to be operated on temperatures on the order of 50mK and stabilized with mK-precision [45], to have fine control on the devices thermal capacitance.

In SNSPDs on the other hand, the detection mechanism is related in part to the electric current in the nanowire, relaxing the requirements on temperature control (in comparison). For SNSPDs, cryogenic setups in the range of 1-2 K are typically sufficient.

2.1.4 Detection mechanism

Different phenomenological models have been reported to describe the detection mechanism in SNSPDs: Hotspot-models and magnetic-vortex-models [25]. They are complementary: the hotspot-model applies especially to high energy photons and large bias currents, while the vortex-model gives better predictions for detection of low energy photons and low bias currents.

The hotspot-model was first proposed by Goltsman [36] and provided a sufficient prediction of most of the detector mechanisms [46]. However, further research showed that it contained distinctly wrong predictions for edge cases such as low-energy photons and dark counts. This led into research of magnetic-vortices [47] which proved successful in predicting experimental curves.

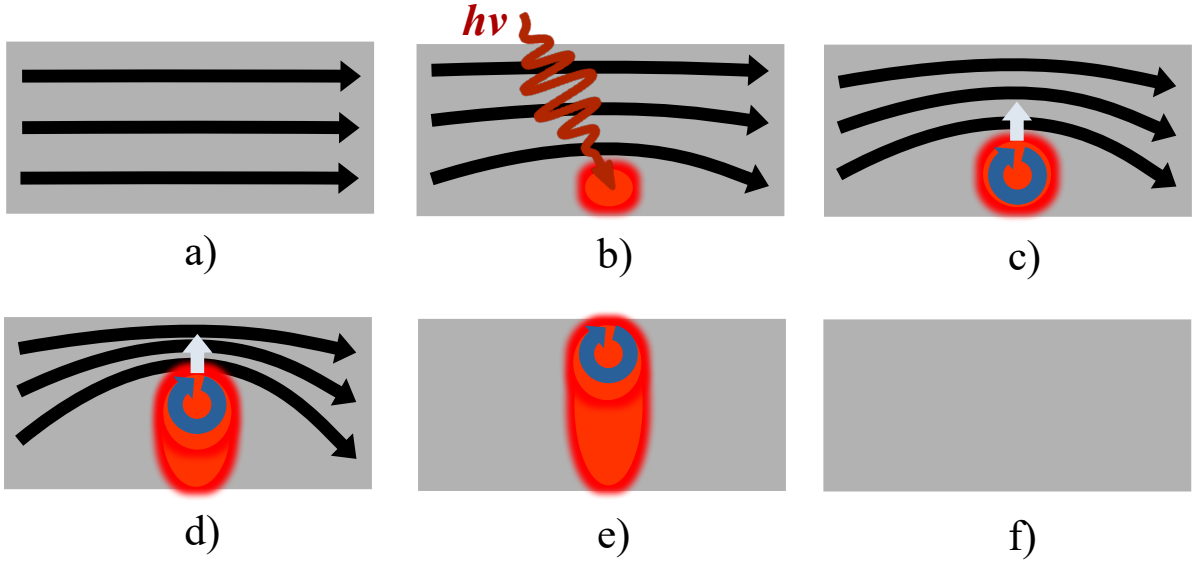

Figure 2.3: Vortex-Assisted Hotspot Model

A thorough discussion of such models and the underlying physics is given in [48]. Here, I sketch the detection mechanism following a vortex-assisted hotspot-model [47]:

1. **Photon absorption**: A photon is absorbed by the superconductor, e.g. via perpendicular illumination or evanescent coupling through a waveguide (b).

2. **Thermalisation**: The photon transfers its energy onto the paired electrons (Cooper Pairs), exciting them into a quasi particles (QP) state. These exited QP can collide with other Cooper-Pairs, exciting them into the QP state as well. A local excess

density of such QP is called a hotspot. QP can loose their energy also via interaction with surrounding phonons, in which case the energy is dissipated into the substrate and the QP thermalize.

3. **Vortex-Unpinning**: Within a hotspot, the excess of QP creates an area of locally suppressed superconducting order parameter. This lowers the energy barrier needed for a vortex crossing. A magnetic vortex is created and unpins from the sidewalls (c).

4. **Vortex-Crossing**: The magnetic vortex experiences a Lorentz Force due to the still flowing current. The Lorentz Force pushes the vortex perpendicular across the nanowire. Along the path of the Vortex superconductivity is further disturbed, expanding the hotspot (d).

5. **Formation of a resistive domain** : As the vortex travels across of the nanowire, the energy released by this crossing can suffice to destroy superconductivity in the area of the hotspot. A resistive domain across the nanowire is formed (e). Further current that flows through the nanowire heats the resistive domains due to joule heating I^2R. This heating effect can increase the local temperature by multiple degree Kelvin.

6. **Signal creation**: The sudden switch of a small section of the nanowire into a resistive state creates a voltage signal that propagates in both directions away from the resistive spot. This voltage signal can be detected with appropriate electronics. The precise extend of the resistive domain depends e.g. on the photon energy and the nanowires inductance (e).

7. **Reset**: The hot resistive domain cools down by dissipating it's energy via electron-phonon and phonon-phonon interactions into the substrate. After some reset time, the nanowire is ready for the next detection (f).

2.1.5 Fundamental properties

I introduce here four of the most fundamental properties of an SNSPD: It's normal state resistance, it's kinetic inductance, it's critical current and it's hysteresis current. These form the basis upon which I can discuss further dynamics.

Normal state resistance

When a part of the nanowire is in it's resistive state, it still allows current to flow, but now against some resistance. This resistance is material-specific, for ca. 5nm thin NbN films for example it lies [25][49] in the range of

$$R_{sq} \approx 300 - 700\ \Omega/\text{sq} \tag{2.1}$$

This is read as "Resistance per square" and means: If a wire is 1µm long and 100nm wide, it can be modeled as being made up out of 10 identical squares, which the current has to

pass sequentially. Each square presents the current a resistance of R_{sq}. If say the specific material has a resistance $R_{sq} = 500\ \Omega$, the wire would have a total resistance of 5 kΩ.

Measuring resistances in squares is useful because the unit is invariant under scaling: If a wire were 2µm long and 200nm wide, it would still consist of 10 squares and have the same total resistance as above. This is because resistance of any wire scales linearly with it's length and inversely with it's width, such that a square offers the same resistance independent of if's scale.

Since one needs some value to work with for estimations, for the rest of this thesis I will use $R_{sq} = 500\ \Omega$ as an average [25] resistance value for 5nm thin NbN wires.

Kinetic inductance

Each superconducting nanowire has a kinetic inductance L_{kin}, which does arise due to the presence and flow of Cooper-Pairs. These charged carriers have mass and show inertia under the influence of external voltages. The inductance for each square of nanowire is

$$L_{sq} = \frac{\hbar R_{sq}}{\pi \Delta_0} = \frac{\hbar R_{sq}}{1.76 \pi k_B T_c} \tag{2.2}$$

where Δ_0 is the superconducting band gap of the nanowire and R_{sq} is it's normal state resistance. The band gap can expressed in terms of the critical temperature T_c via $\Delta_0 = 1.76 k_B T_c$ by the BCS theory. With e.g. T_c =10 K and R_{sq} from above I get an inductance of $L_{sq} = 69$pH/sq. If a wire were to have 10 squares, this would result in a kinetic inductance $L_{kin} = 690$pH.

A different derivation of the kinetic inductance allows to see the influence of the geometry more directly. For a nanowire with length l, width w and height h, the kinetic inductance is [15]:

$$L_{kin} = \frac{m_e}{2ne^2} \frac{l}{w \cdot h} \tag{2.3}$$

where m_e is the electron mass, e the electron charge, and n the electron density. The factor two arises due to electrons flowing as Cooper pairs. It can be seen that the kinetic inductance scales in proportion with the length of the nanowire and inversely with it's height and width. This allows to design nanowires with specifically chosen inductances.

Very close inspection of theory and experiment show that the inductance also slightly varies (by up to 10 percent) with the amount of actual current flowing in the nanowire [45].

In our group, a slightly higher value of $L_{sq} \approx 0.5$nH/sq was experimentally found for our NbN films. I will use this higher value for further estimations in this thesis, as it's assumed to be closer to the actual films I work with.

The inductance L in an electrical circuit determines and limits how fast a flowing current can change its magnitude and direction. Mathematically this is expressed via $dI/dt = U(t)/L$. Most inductors in electronics get this inertia via a magnetic field created by a spiral wire geometry.

Such a spiral geometry however is almost impossible to mimic with a flat superconducting film. It is thus interesting to note that these flat superconducting wires still have a material-intrinsic inductance through their Cooper-Pairs, independent of any larger-scale geometry.

Critical current

The critical current I_c of a nanowire is defined as the maximum current it can support in it's superconducting state. Each superconducting material has some intrinsic critical current density j_c, which is the maximum current it can support per crossection of wire. In a nanowire of width d and height d this relates the nanowires critical current and the materials critical current density via:

$$j_c = \frac{I_c}{wh} \tag{2.4}$$

In figure 2.4 an IV-Curve of an SNSPD is displayed, in which the value of the critical current I_c can be seen by the sudden jump into resistivity. The biasing current was ramped up from zero to some maximum value and then ramped down again.

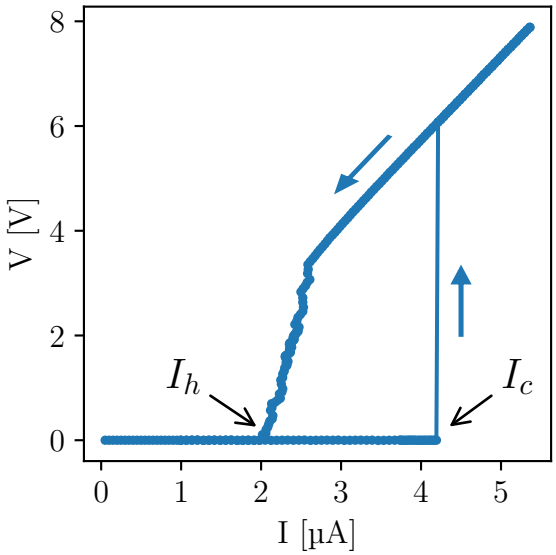

Figure 2.4: IV-Curve of an SNSPD, with annotated critical current I_c and hysteresis current I_h. The blue arrows indicate the progression of the scan.

The critical current density is temperature-dependant. The exact relationship $j_c(T)$ can be calculated via the Ginzburg-Landau theory [50], given by the equation

$$j_c(T) = j_c(0)\left[1 - \left(\frac{T}{T_c}\right)^2\right]^{3/2}\left[1 + \left(\frac{T}{T_c}\right)^2\right]^{1/2} \tag{2.5}$$

where $j_c(0)$ is the critical current density at very low temperatures ($T \ll T_c$). For NbN, this critical current density is ca. $j_c(0) \approx 6$ MA/cm^2 [51]. The exact value per material depends also on the quality of the deposited film.

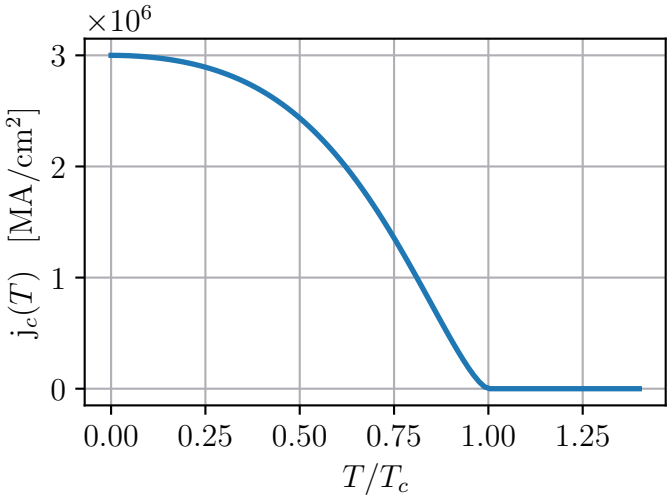

Figure 2.5: The Ginzburg-Landau-Relation for the critical current density $j_c(T)$

From the Ginzburg-Landau-Relation it can be inferred that for low enough temperatures (approx. $T \leq 0.25T_c$) one can approximate the critical current density to a good degree as constant. For higher temperatures instead, the gradual decline in critical current density should be considered.

Experiments in our group showed that especially very thin nanowires don't exactly follow the relationship predicted by equation 2.4. Instead, there exists, among else, a small offset for very narrow wires. This is believed partly due to proximity effects to the substrate, as well as fabrication imperfections such as rough sidewalls. For low temperatures, $T < 0.25T_c$, our group [15] found the following fitted relationship for ca. 5nm thin NbN nanowires:

$$I_c(w) \approx -5\ \mu\text{A} + w \cdot \frac{10\ \mu\text{A}}{60\ \text{nm}} \tag{2.6}$$

which can also be inverted for the use the other way round, then reading

$$w(I_c) \approx \frac{60nm}{10A} \cdot (I_c + 5A) \tag{2.7}$$

For the remainder of this thesis I will use this experimental relationship as a reference when needed to relate critical currents to widths.

Hysteresis current

The hysteresis current I_h marks the current at which the nanowire returns from the resistive back into the superconducting state, annotated in figure 2.4. The transition is due to

a electrothermal effect [52]: Once a nanowire switches to the resistive state, it's resistive domains are heated up via joule heating.

As long as a high current flows such that this heating is larger than the dissipation into the substrate, the nanowire stays at an elevated temperature and in a resistive state. This persists even if the current is reduced below the critical current I_c, giving rise to the hysteretic behaviour.

The hysteresis current I_h marks thus the threshold at which the joule heating drops sufficiently low such that the nanowire cools down, and returns to it's superconducting state. It can be analytically approximated as the current for which the following balance is fulfilled [53]:

$$\rho I_h^2 = 2h_c(T_c - T_s) \tag{2.8}$$

where ρ is the normal state resistance of the nanowire per unit length, h_c is the thermal boundary conductance between nanowire and substrate, T_c is the critical temperature of the nanowire and T_s the substrate temperature. The hysteresis current is thus dependent on the thermal environment surrounding the SNSPD.

This poses a hard requirement for any interfacing circuit to an SNSPD: The circuit must be designed such that at some point after photon detection the current through the nanowire falls below I_h, as otherwise the nanowire does not return to superconductivity. I_h in turn depends on static properties of the nanowire (ρ and T_c) as well as on the thermal interface to the substrate (h_c and T_s).

2.1.6 Circuit dynamics

We can now discuss the circuit dynamics after a photon absorption. The circuits dynamics arise because an SNSPD is embedded in an electrical circuit that delivers the necessary bias current and passes through the detection signal.

Equivalent electrical model

To help theoretical analysis and simulation, SNSPDs can be expressed via an equivalent electrical model. One of the first proposed models was by Kerman et al. [24], shown in figure 2.6. The kinetic inductance of the SNSPD is modelled via an fixed inductor and the transient appearance of a resistive domain via a fixed resistor and a switch. Changing the state of the switch in time allows to model the change between superconducting and resistive state of the nanowire.

Interfacing Circuit

Figure 2.6 not only shows the SNSPD, but also a basic interfacing circuit: A current source that delivers a constant bias current I_0 to the SNSPD, and in parallel to the SNSPD a load impedance of 50Ω, modelling the typically 50 Ω-matched impedance of any transmission line. This is a basic possible interfacing circuit and often employed [46][53].

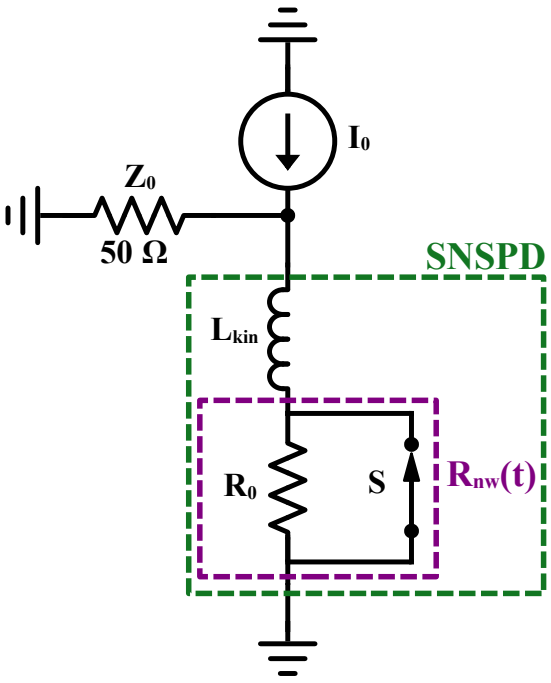

Figure 2.6: Equivalent Electrical Model of an SNSPD plus surrounding interfacing circuit

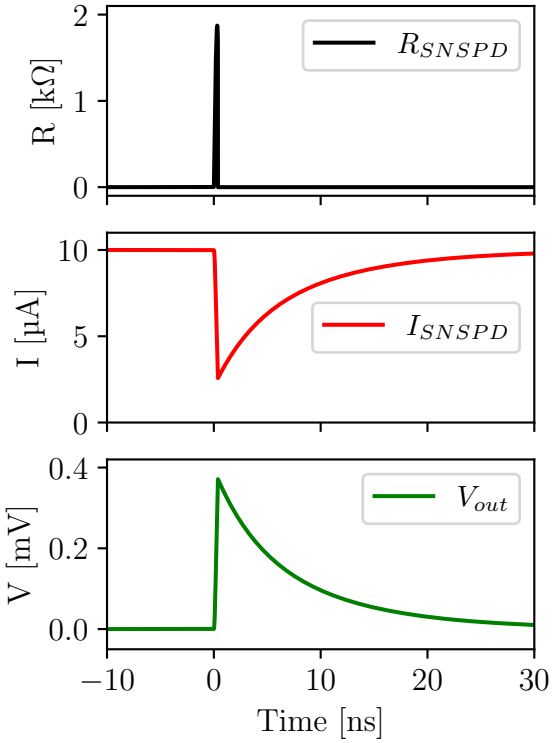

Figure 2.7: LTspice simulation of an SNSPD-Click after photon absorption

Photon detection cycle

I now present a first view into the interplay between SNSPD and interfacing circuit after photon absorption. A simulation of the interfacing circuit is given in figure 2.6. To simulate SNSPDs, I use the SNSPD-Library developed by the group of Berggren [54] for LTspice. Further details on the software are given in section 4.1. The simulation results with a photon absorption at t=0 are shown in figure 2.7, with which refer to to describe some main dynamics:

- **Resistive domain size**: After the photon absorption the SNSPD develops quickly a resistive domain, on the order of 1-2 kΩ.
- **Redistribution of current**: As soon as the resistive domain has formed, the biasing current redirects to a large part away from the SNSPD and into the load impedance Z_0, as it offers a much less resistive pathway to ground.
- **Superconducting reset** Once the current in the nanowire is reduced below it's hysteresis current I_h, it cools down and returns to it's superconducting state.
- **Output voltage**: A voltage signal of approx. $V_{out} = I_0 \cdot Z_0$ is created over the load, with magnitude on the order of 0.5mV. This is the signal that can be detected by further electronics.

- **Detection reset time**: The bias current does not immediately return into the nanowire, but only after some characteristic time delay given by $\tau = L_{kin}/Z_0$. The SNSPD is only sensitive to a next photon once it's current is close to the original bias current, thus the delay τ sets a limit to the count rate of the detector.

2.1.7 Latching

As the detection reset time of the SNSPD is given by the time constant $\tau = L_{kin}/Z_0$, a natural attempt would be to just increase Z_0 to shorten this downtime. This approach is indeed possible, but only to some degree. In figure 2.8 an SNSPD click with four different readout loads Z_0 ranging from 100 to 400 Ω is simulated, using the standard circuit from figure 4.1.

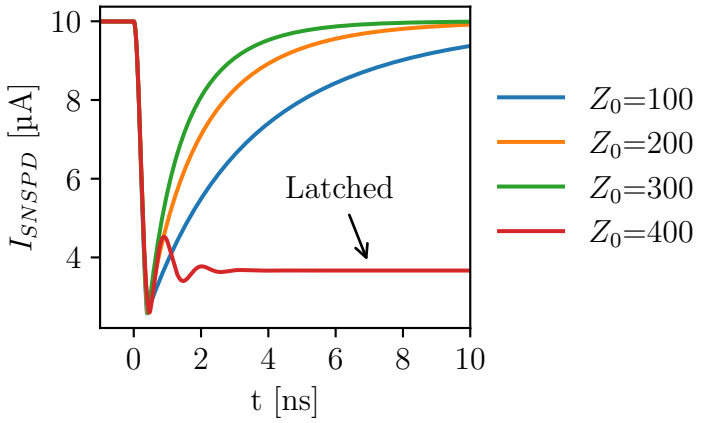

Figure 2.8: The resetting dynamics of a nanowire under different load impedances. The high load impedance of $Z_0 = 400$ Ω leads to permanent latching, impeding any further photon detection.

For load impedances up to $Z_0 = 300\Omega$, the detection reset time is indeed shortened. However, if the load is pushed further to around $Z_0 = 400\Omega$, somethings qualitatively different happens: The circuit latches [52]. The current returned so quickly into the SNSPD that the resistive domains didn't have enough time to cool down, but instead are heated now persistently by joule heating. This traps the nanowire in a permanent resistive state, where it is not sensitive to any new photons.

When designing any new SNSPD readout circuit, it is thus absolutely necessary that the bias current at some point in time drops below the hysteresis current I_h of the SNSPD, such that it can reset back into it's superconducting state [55].

A note: latching can also be influence by other factors such as intense photon irradiation, which is encountered especially at high photon count-rates [56]. The photon irradiation can increase the bias current due to excess charges in the readout circuit, leading to latching behaviour that would be absent at lower photon counts. In scope of this

thesis however, I restrict my analysis of latching to electronic and thermal effects, i.e. in the limit of low photon counts.

2.1.8 Further details

I comment here on an adjacent topic about nanowires which do not fit directly in any of the above topics, but which is relevant.

Hotspot growth

The resistive hotspot in an SNSPD grow and relax dynamically [53], which can be described analytically. If a current I close to I_c flows through an SNSPD, and the SNSPD already has a resistive hotspot, then the spatial growth velocity of this hotspot can be approximated via [57] :

$$v_{HS} = \frac{2}{cw}\sqrt{\frac{\kappa R_{sq} I^2}{d(T_c - T_{sub})}} \tag{2.9}$$

where c is the specific heat of the nanowire, w is its with, κ it's thermal conductivity, R_{sq} the normal state resistance, d the film thickness, T_c the critical temperature of nanowire and T_{sub} the substrate temperature. The factor two arises because the hotspot has two boundaries [57]. For NbN, the thermal parametes are $c = 4400$ J/m^{3}K and $\kappa = 0.108$ W/(mK)[57]. If one assumes a typical SNSPD with d =5nm, $w = 100$nm, $R_{sq} = 500\Omega$/sq, T_c =10K, T_{sub}=2K and remaing bias current I =6µA after an initial hotspot has formed, we get a hotspot growth velocity of

$$v_{HS} \approx 1.0 \text{ µm/ns} \tag{2.10}$$

That is, the resistive domain grows by one µm alone the nanowire along every nanosecond. If the SNSPD is say 100nm wide, then ten nanowire-squares turn resistive every nanosecond. With R_{sq} =500 Ω this leads to a change in resistance of $dR/dt = 5\text{k}\Omega/\text{ns}$.

Further details on hotspot dynamics can be found e.g. in the review by Gurevich [58]. One area were the growth speed of hotspot had to be explicitly taken into account was e.g. in fast superconducting microwave-switches [59].

2.2 Intermediate signal amplification

The typical voltage signal created by an SNSPD is on the order of 1mV. This is too small to detect with typically available hardware such as oscilloscopes. Thus, the signal is almost always amplified by some means, into the regime of around 100mV [17].

One popular method for such amplification are low-noise electronic amplifiers [60]. They are commercially available and can be inserted into the signal line right before the detection electronics. However, they also introduce noise in the signal, which can degrade detector performance [61].

In this section, I present three complementary techniques besides commercial amplifiers that allow to amplify signals of SNSPDs: Cascading, Impedance-Matching and On-Chip-Switches. All three methods exploit some specific property of SNSPDs (or superconductive elements in general). This can also give insight into the degrees of freedom that are possible in interfacing SNSPDs.

Cascading

Cascading is a type of on-chip circuit design where an optically coupled SNSPD is connected to parallel superconducting wires with the aim of enhancing the response of the sensing element [62]. An exemplary circuit is sketched in figure 2.9 where three identical SNSPDs are added in parallel. The motivation behind this arrangement is the increase in total bias current I_b. The output voltage after a detection is approximately given by $V_{out} = I_b \cdot Z_0$, an increase in bias current (approximately) linearly increases the output voltage. Since a single SNSPD can only support current up to order 10µA, parallel superconducting elements are needed to achieve higher overall bias current.

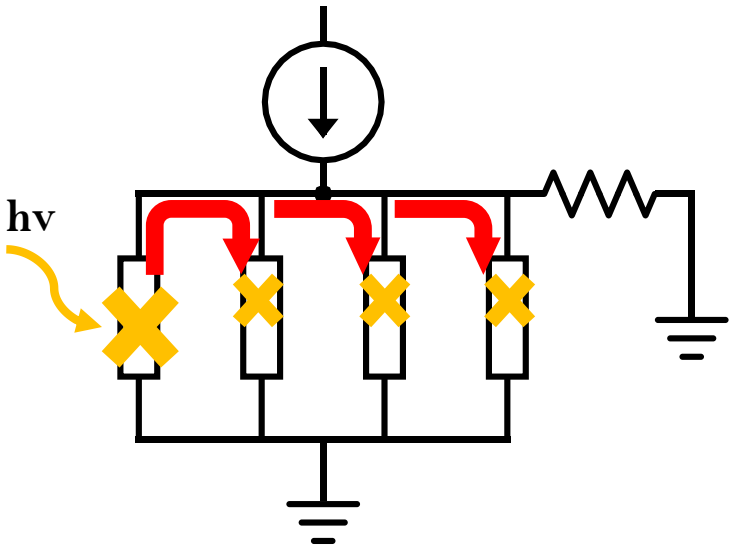

Figure 2.9: Cascading with 4 SNSPDs in parallel

To achieve a cascading effect, all elements must be initially biased just below their respective critical currents. When one SNSPD triggers due to a photon, it's current gets redistributed to the other elements (still superconducting at that moment). If this redistributed current is then larger than the difference between bias current and critical current of the respective elements, they exceed their critical current as well and become also resistive. This leads ideally to a cascading effect until in short succession all involved elements are resistive.

A cascading of $N = 5$ parallel elements was demonstrated in 2007 [62], called superconducting nanowire avalanche photon detectors (SNAP). Further works reported e.g.

$N = 12$ and $N = 24$ elements [63] [64]. Such a design requires that all wires have the same critical current I_c, on which fabrication imperfections impose a limit. It was reported that already beyond $N = 4$ parallel elements difficulties appeared regularly [65]. To relax such fabrication requirements, Binary Tree-Based cascading was proposed, where cascading happens in distinct hierarchies [65]. In some circumstances cascading can also be a harmful side effect that needs to be actively prevented [66].

Impedance matching

Electrical Impedance extends the concept of resistance to alternating currents, and can describe frequency-dependent phenomena in electrical circuits (ref). The Impedance Z of a circuit element is given by

$$Z = R + jX \tag{2.11}$$

where R is the dissipative resistance to DC currents, j is the imaginary unit, and X is the reactance of the circuit element. The reactance is (in general) frequency-dependent. To note the most fundamental circuit elements: The impedance of Capacitors is $Z_C = 1/jwC$, the Impedance of inductors is $Z_L = jwL$, and the impedance of Resistors is $Z_R = R$. Transmission lines (such as coaxial cables) can be designed such that they present, from some lowest frequency point onwards, a constant frequency-independent impedance Z_0.

When two circuit elements with different impedances Z_1 and Z_2 are connected to each other, an incident wave to the interface is partly. The fraction of the reflected signal is given by

$$\Gamma_{12} = \frac{V^-}{V^+} = \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{2.12}$$

where V^+ is the voltage of the incident wave and V^- that of the reflected wave. It can be seen that no reflection is only realised when the circuits have the same impedance. To prevent such reflections, most high-frequency electronics worldwide is standardized on a single impedance of $Z_0 = 50\ \Omega$. For special cases, impedances of 30 Ω and 70 Ω can also be found.

For SNSPDs, numerical simulations show that during a detection event they have an impedance on the order of $Z_S = 3$ kΩ [67]. Interfacing such an SNSPD with a coaxial cable results in high reflection losses, diminishing any voltage signal from a detection event and limiting the transmitted voltage to approximately $V_{out} = I_b \cdot 50\Omega$.

A device that can interface between different impedances is an electrical taper [68]. It is, in essence, a conductive wire that is wide at one end and narrow at the other end, with a smooth transition of it's width in between. One popular design choice is the Klopfenstein-Taper [69].

At the narrow end the taper has a high impedance Z_H and at the wide end it has some lower impedance Z_L, which both are determined (predominantely) just by this very geometry. The transition in the width has to be stretched out over a long enough length such that the electrical signals don't notice the gradual change in impedance [70].

By using such an impedance taper between SNSPD and coaxial cable, the voltage

amplitude of the signal can be increased by the factor [71]

$$G = \sqrt{\frac{Z_H}{Z_L}} \tag{2.13}$$

which would result for an SNSPD in a voltage signal increased by a factor ∼8.

In regards of integrated photonics, one disadvantage of such tapers is their large footprint, which was reported up to 5mm x 3mm to interface a single SNSPD [72]. When a high density of detectors is desired, this prevents interfacing each single one with with it's own taper.

Voltages response of lumped elements

Knowledge about the properties of circuit-elements can help in the design of circuits, as we have just seen in the example of the Impedance-Matching. Here I want to expand on this and give a minimal intuition into how voltages within a circuit form. For the three basic circuit elements Resistor R, Capacitor C and Inductor L, the voltage V_i that falls off over these elements is given by [73]:

$$V_R(t) = I(t)R \tag{2.14}$$

$$V_C(t) = \frac{Q(t)}{C} \tag{2.15}$$

$$V_L(t) = L\frac{dI(t)}{dt} \tag{2.16}$$

For a resistor, the voltage is given by the instantaneous current $I(t)$ flowing through it. For a Capacitor, the voltage is given by the total charge $Q(t)$ that has accumulated at it up to that point. For an Inductor, the voltage is given by the instantaneous *change* in current $dI(t)/dt$ flowing through it.

Each of these elements develops it's voltage over a different mechanism, and with different time scales involved. This knowledge might help to design circuits where the voltage of a specific element is maximized at some point in time. Which would be, for the outside observer, nothing else but also a signal amplification.

Thermal switches

Heat applied next to a superconductor can directly destroy it's superconductivity if the temperature reached is beyond the critical temperature T_c of the superconductor. According to McCaughan [74], such a heater idea was first demonstrated experimentally in 2003, coined a "Hot-Phonon-Switch" [75]. Figure 2.10 gives a sketch of such a heater setup.

Designs of with the heating element next to the superconductor [76][77] as well as the heating element on top of the superconductor [78] have been shown, with comments mentioning the need for the layered approach due to slow heat transfer in the planar design [78].

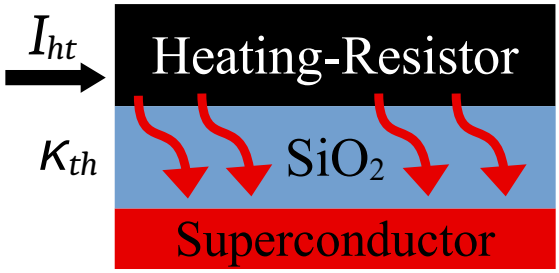

Figure 2.10: Sketch of a 3-layer thermal switch

A thin buffer layer is required between the heating element and the superconductor for layered switches, to isolate electrically. Employed materials for such a layer have been 10nm SiO [75], 25nm SiO [21] [79], 12nm αSi [80], and 190nm SiO [81]. The last higher value was choosen specifically to reduce electrical capacitive crosstalk.

Thermal switches have the interesting property that the controlling current in the heating unit is electronically isolated from the controlled bias current in the nearby superconductor [80]. This allows for flexible circuit design and new coupling techniques [82] [21].

One application making use of this electrical isolation is the coupling between circuits with vastly different impedances. A vertically stacked 3-Layer-Switch allowed to transfer a signal thermally from a low-impedance circuit (50 Ω) to a high-impedance circuit (400kΩ), resulting in a controllable voltage of 1.12 V in the second circuit [78]. This did not require any impedance matching, as electrical contact was completely bypassed. However, the response time can be increased, as thermal coupling is considerably slower than any electrical coupling.

Apart from photons, large electrical currents and heat, superconductivity can also be disturbed via a bit more exotic approaches. I want to mention here three in passing. Capacitor-coupled high-frequency gating signals that periodically drive the bias current beyond the critical current [59], creation of ballistic phonons via excess voltages of 4V and more [83] [84], and injecting non-equilibirum quasiparticles from one superconductor to a second nearby superconductor via tunneling effects [85] [86].

2.3 Readout of SNSPDs

In this last section I present the approaches employed in transmitting signals from cryogenics chips to the outside world, the last step of a signal registration. A main bottleneck in many schemes is the thermal load introduced by any sort of interfacing, limiting the readout capabilities of many devices in parallel [17].

I introduce first some basis of electronic readout, then a techniques that allow to address multiple detectors via a limited amount of wires, and present in the end optical

readout as qualitative different scheme for interfacing cryogenic chips.

2.3.1 Electronic readout

Since SNSPDs create a voltage signal, the most straightforward approach to carry this signal out of the cryostat is via some continuous electrical wiring. This is indeed the default approach taken in virtually every setup, it is robust and easy to implement.

A general pathway for electronic readout is similar to the following [87]: The signal from the SNSPD (or any cryogenic device) first travels within the chip until it reaches a bondpad. Wirebonds transport the signal to a nearby surrounding printed circuit board (PCB) installed in the cryostat. Coaxial cables connect from there to the walls of the cryostat, where feed-through connectors pass the signal to the of the cryostat. There, low-noise amplifiers are often employed to to increase the voltage signal from ca. 1mV to around 100mV [17], a voltage level which can then be registered with readout-electronics such as oscilloscopes, and digitized.

Due to the fact that each coaxial cable in such a setup is both in contact with room-temperature (∼300K) and with the cryogenic stage (∼1K), the number of coaxial cables is restricted by the cooling powers of the cryogenic system. As an estimate, each coaxial cables transports ca. 1 mW of heat into the cryogenic system [88]. Small cryostats can handle on the order of 10 mW and larger cryostats on the order of 100 mW heat input, but in any case, this limits the amount of coaxial cables to the order of 100.

A similar argument concerns cryogenic amplifiers. One can install electronic amplifiers inside the cryostat to amplify the signal closer to the source. This has benefits such as reducing the Johnson-Nyquist noise, i.e. thermal noise [60]. However, even low-power amplifiers dissipate power on the order of 5-10 mW, limiting their number to only a few [61] [89].

To given an order of magnitude, the attenuation in cryogenic cables is ca. 3dB/m for frequencies in the range of 1-10 GHz [90] [91] [92]. The 3dB-attenuation marks the point at which a signals amplitude is reduced to half it's initial value. Since also noise increases with signal frequency, a typical bandwidth that is used to interact with SNSPDs is on the order of 1 GHz.

Large-scale pixel-array readout

There is an ongoing effort in increasing the number of detectors per chip, because at some point, when scaling reaches into the thousands of detectors, this would allow to turn the chip into a camera. I present this topic also because it allows to observe trade-offs and limits of electronic readout particularly well.

Specific areas of interest for SNSPD-based cameras are in the deep-UV for astronomical applications [21] as well as the IR for biomedical imaging [93]. In such arrays, detectors are also referred to as pixels, which I adapt for this section.

To read out a large number of pixels (100-100k) with only few available coaxial cables (10-100) requires techniques to multiplex the detector signals, such that for each signal travelling through a coaxial cable the pixel of origin can be inferred [17]. I give a short summary of the development of such techniques, a condensed list is in table 2.1.

Table 2.1: Development of large-scale SNSPD readout techniques

Year	**Technique**	**Scaling**	**Pixels (NxN)**	**Readout Wires**	**Ref.**
2007	Direct readout per pixel	N^2	2 (2x1)	2	[94]
2013	Direct readout per pixel	N^2	12 (3x4)	12	[95]
2014	Direct readout per pixel	N^2	64 (8x8)	64	[96]
2014	Electric c.+ Time-tagged	$2N$	4 (2x2)	4	[97]
2017	Time of flight (TOF)	const.	590 (1)*	2	[98]
2019	Electric c.+ Time-tagged	$2N$	1024 (32x32)	32	[99]
2020	Thermal c.+ Time-tagged	$2N$	16 (4x4)	8	[82]
2022	Thermal c.+ TOF	const.	1024 (32x32)	8	[21]
2023	Thermal c.+ TOF	const.	400,000 (500x800)	8	[16]

*590 effective pixels within a single long detector

Early work on large-scale pixel arrays started with direct readout of two pixels, which led to a maximum count of 64 pixels [94][96]. Further scaling was prohibitive, as for NxN pixels, N^2 wires were required.

The number of wires could be qualitatively reduced with the introduction of electrical rows-column coupling, which together with a time-tagger allowed to read out NxN pixels with only $2N$ wires, leading to up to 1024 addressable pixels [97][99].

Thermal instead of electrical row-column coupling was subsequently developed, which greatly reduced electrical cross-talk in large arrays [82]. By extracting spatial position via Time-of-flight measurements (as opposed to time-tagging), the number of required wires could be reduced further to a constant value (of 8 wires), independent of pixel count [98][21]. Via this combination of multiplexing techniques, all major theoretical roadblocks regarding scaling were eliminated.

The at present largest reported detector-array consists out of 400.000 pixels, all addressable via 8 wires [16]. The maximum count rate was up to ca. 100kHz, meaning that each single pixel could be read out on average once every 4 seconds.

2.3.2 Optical readout

Since electronic readout can be scaled up to large arrays only at the cost of reduced readout speed per detector (as seen in the previous section), new approaches for readout are being explored. One promising candidate is optical readout, based on interfacing the cryogenic chip through optical fibers via an external laser light [18]. Research in this area is motivated by the lower thermal load and higher bandwidth that optical interconnects can potentially offer [22].

I introduce the electro-optic-modulator, the core device that provides the link between electric and optic domain, and the present some recent developments within the field of optical readout.

Electro-optical resonators

An electro-optic modulator (EOM) is a device that allows to modulate passing light via applying a voltage to the modulator. It is based on the electro-optic effect, also called pockels-effect [100], which is the change of optical properties of a material in response to an external electric field.

By applying a voltage to an EOM, the refractive index of the electro-optic material is changed slightly. Light passing through experiences this change in refractive index, which shifts it's phase. This phaseshift can then be exploited in various arangements to control the amplitude and direction of the light.

A popular electro-optic material is $LiNbO_3$, which has an electro-optic coefficient of ca. 27pm/V [101]. Under the influence of an electric field, the polarized charges in it's crystal lattice rearrange spatially (slightly), changing the refractive index of the material.

In integrated photonics, the electro-optic effect of $LiNbO_3$ can be exploited e.g. via Racetrack-Resonators [19]. These are closed-loop oval-shaped waveguides surrounded by electrodes. When a voltage is applied, the change in refractive index shifts the optical resonance frequency of the resonator. When light of a specific frequency is guided close to such a resonator, the resonator can be tuned to either absorb the light (if in resonance) or ignore it (if out of resonance). This allows to control the amplitude of the bypassing light via the applied voltage. For $LiNbO_3$-Racetrack-Resonators, reported modulation efficiencies have been for example 3.2pm/V [102] and 8.5pm/V [103].

Recent developments in optical readout

A general setup for optical readout follows these steps [22]: First, an external laser is coupled from room-temperature near to the chip via optical fibers, and is then coupled onto the chip via optical grating couplers. Integrated waveguides then guide the light within the chip where it is modulated by an integrated EOM. The EOM is controlled by the on-chip electric signals of interest, imprinting their signal onto the light. Finally, the now modulated light is coupled back out of the chip and guided again via fibers to some external detector at room temperature. By measuring the modulation, information originating from the chip can be retrieved.

This interface allows to transmit signals without any physical wires contacting to the chip. The laser light itself (and potentially any modulators on chip) do bring some thermal load as well, but compared to coaxial wires it is ca. two orders of magnitude lower [18]. Furthermore, strategies such as wavelength division multiplexing could be employed that would increase the bandwidth and allow to address multiple detectors on-chip at the same time. An example of a "photonic link" was recently reported in [104] with optical data

transfer rates in the GHz-regime.

A demonstration of optical readout specifically of SNSPDs was presented by de Cea et al. in 2020 [22]. A CMOS-integrated photonic ring-modulator was employed for the modulation, which provided a resonance shift of ca. 700pm/V. A device with such a high shift value was necessary because the SNSPDs provided only an output voltage of ca. 2mV. In combination, a resonance shift in the ring-resonator of ca. 1.4pm could be achieved after an SNSPD click, reducing the amplitude of a transmitted external laser temporarily by ca. 1%. This change in amplitude was then resolved by external photo detectors.

The setup was limited to the detection of UV Photons because only for those high-energy photons the detectors could generate a strong enough voltage signal. Additionally, the detector-design led to rather slow reset times on the order of 1µs.

Sketch of the proposed setup within this thesis

At the end of this chapter a visual sketch of the proposed optical readout scheme is given, as motivated and introduced earlier (section 1.2). The sketch is given in figure 2.11. An SNSPD would be connected via a yet-to-be determined interfacing circuit to a $LiNbO_3$-Racetrack-Resonator EOM, fabricated next to an integrated waveguide. When the SNSPD absorbs a photon, the voltage signal is transmitted (and ideally, amplified) via the interfacing circuit to the EOM. The voltage shifts the optical resonance frequency of the EOM, changing the strength with which the readout laser is coupled into the resonator ring. The resulting change in the laser light amplitude can then be registered by an external detector outside the cryostat.

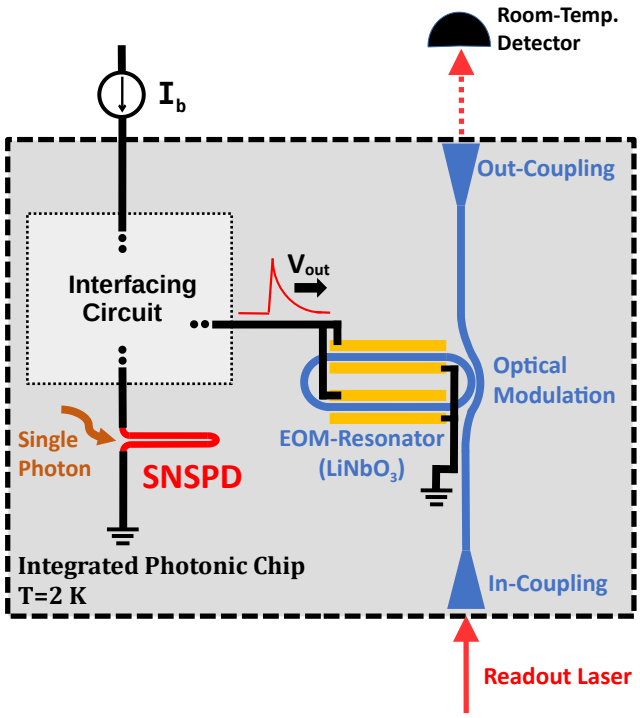

Figure 2.11: High-Level sketch of the optical readout scheme which I work towards in this thesis.

Chapter 3

Simulating a cryogenic thermal switch

In this chapter I simulate the transient heat distribution of a cryogenic thermal switch, as presented earlier 2.2. The Motivation stems from the potential application of such a switch to the interfacing circuit between SNSPD and EOM, where it could provide during the detection cycle a controllable resistance and thus a re-configurable circuit.

Previous work about thermal switches (background 2.2) showed that they were applied in similar cryogenic environments to ours, further motivating a potential integration.

I begin by introducing the simulation tool, and then present all required thermal parameters. Then I present the geometries of the switches to simulate and their specific simulation conditions. Finally I present the simulation results of the switches for different heating currents and material combinations and discuss the results.

3.1 Simulation tool

Comsol

I do the transient thermal simulations via COMSOL Multiphysics, a commercial physics simulation software. It allows to simulate a wide range of physical phenomena, such as electromagnetism, structural mechanics or fluid flow. I use the module for transient thermal heat transport.

The simulation is based on the finite-element-method (FEM), where differential equations governing the physical interactions are solved numerically. To this end, the desired physical problem defined by the user is discretized both in space and in time. The geometry is divided it into a mesh of many small but finitely sized domains, and the desired time span is divided into small finite time steps. The differential equations are then evaluated in discrete time steps and on the discrete geometric domains, approximating the real continuous dynamics. To this end, both the step size and the spatial mesh size need to be chosen small enough such that the discretization does not introduce significant artifacts in the simulation result.

As an input, Comsol requires the the thermal parameters of all involved materials. For our temperature range of interest (cryogenic temperatures in the regime 2-20K), such

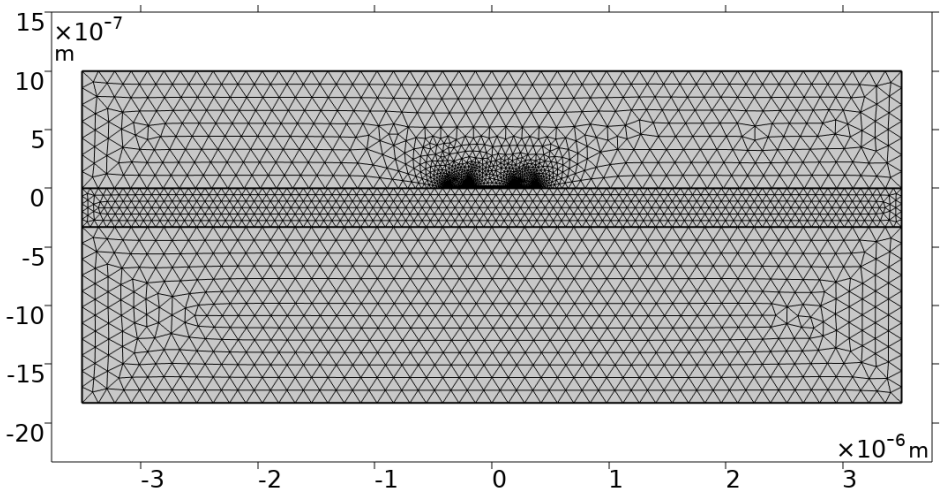

Figure 3.1: A view of the 2D-Mesh employed in the simulations. Near geometries of smaller scale the mesh is automatically adapted to finer resolution, to treat the small scales appropriately

material parameters were unfortunately not readily available by any internal library. Thus, I had to collect these parameters from literature and convert them to a format amendable to Comsol.

3.2 Material properties at cryogenic temperatures

The materials which I want simulate can be sorted into groups, each dictated by it's own considerations:

- **Si, SiO_2, $LiNbO_3$, NbN**: The constituents of the material stack required for this chip.
- **SiN**: The default waveguide material on most chips where $LiNbO_3$ is not required. Prominent enough that I want to include it for completeness.
- **Au, Pd, Ti**: Metals that are available for deposition by the fabrication process. Useful as electrical connections, electrodes and on-chip resistors.

Some of the materials are required to be simulated because they will be part of any fabricated chip, while others are optional. The optional ones were chosen by availability of fabrication. In the case of SiN, it's simulation would not be directly necessary to this thesis, but since it is part of many other photonic designs, for which cryogenic simulations could also become interesting, I include it here in for any future reader working with SiN.

For each of these material, Comsol requires the following thermal properties

- its heat capacity c

- its thermal conductivity κ
- its thermal boundary conductivity G
- its electrical resistivity ρ (for the metals and NbN)

A sketch of the physical meaning of the thermal parameters and their involved units is given in figure 3.2. While heat capacity c and thermal conductance κ might be familiar to most readers, thermal boundary conductance G might be not. Each parameter is now shortly introduced and it's physical particularities discussed. I comment on the discovered literature results and the chosen parameters values.

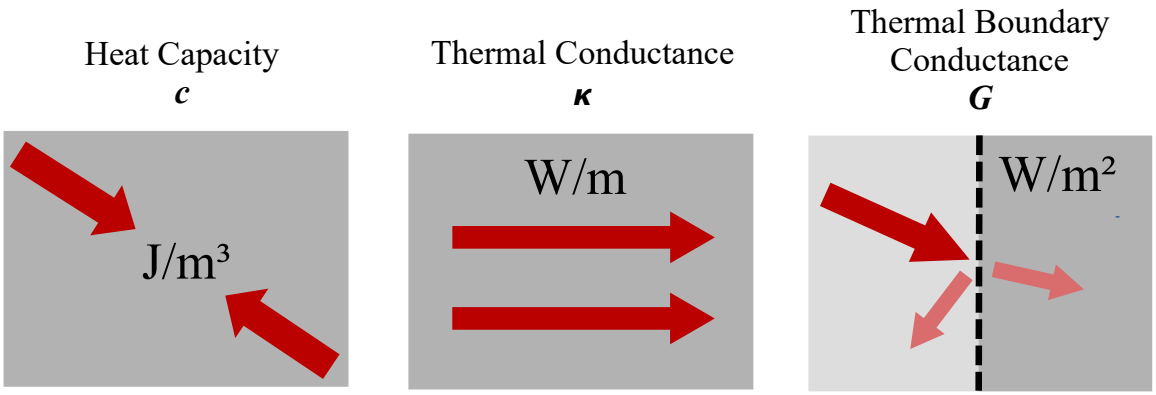

Figure 3.2: The thermal properties required for simulation

Simulation at cryogenic temperatures

Some preliminary comment on the strategies applied in the next sections:

I simulate the thermal properties of our system in the temperature range from 2 and 20K. 2K is the temperature at which our experiments will be performed, while 20K is the maximum temperature reached by the simulated heating elements given by the maximum heating current chosen for simulation.

Many of the popular and simple theoretical models that accurately describe thermal parameters in the room-temperature regime are no longer reliable at cryogenic temperatures [42]. At low temperatures, new exotic and less well studied electronic and thermal transport phenomena appear, requiring more sophisticated models. However, following and using these models to extract the thermal parameters would be beyond the scope of this thesis.

I will rely mostly on published experimental data. Multiple sources are referenced where available, giving some more statistical security to the chosen values. However, finding multiple sources was not always possible. When no direct data is available for a specific parameter, I try to derive it from the other available parameters for a given material, following the steps that are reported in literature to calculate such missing parameters.

For each extracted parameter I give the corresponding temperature range on which the parameter value is based on.

3.2.1 Heat capacities

Heat capacity c is given in units J/m^3K and specifies how much energy a material can absorb in a given volume before it's temperature increases by 1 Kelvin. The most popular way to model heat capacities is via the Debye-T^3 Model [105], which assigns each material a Debye-Temperature Θ_D, from which the heat capacity can then be calculated via the prominent formula

$$c = \frac{12\pi^4}{5}\left(\frac{T}{\theta_D}\right)^3 \tag{3.1}$$

However, for the low temperatures we are dealing with here, the Debye-Model starts to break down. To quote one paper, referencing the temperature range below 10K: "the calculated Debye specific heat is more than an order of magnitude less than the total specific heat, indicating that in this temperature range C is completely dominated by nonacoustic modes" [106].

The collected heat capacities from reported experiments in literature for every material are listed in table 3.1. It turned out that SiN and SiO were by far the most popular materials amongst our selection, providing ample data. For the metals, the electronic heat capacity must be included in tandem with the phononic contributions. This might be one of the still more widely known low-temperature phenomena [105].

Table 3.1: Heat capacities

Material	Heat Capacity c	Range	References*
SiN	$279\,J/m^3K^2$	3-10 K	[106], [107] [108] [109]
NbN	$1.03\,J/m^3K^4$	3-16 K	[79], [110] [23]
SiO	$5.24\,J/m^3K^4$	0.1-10 K	[111], [112] [113] [106] [114] [115] [116] [117]
LiNbO	$6.28\,J/m^3K^4$	2-20 K	[118],[119]
Pd	$c_{el} = 1056\,J/m^3K^2$ $c_{ph} = 10.8\,J/m^3K^4$	2-18 K	[120], [121]
Ti	$c_{el} = 320\,J/m^3K^2$ $c_{ph} = 2.47\,J/m^3K^4$	3-16 K	[79]

For Pd and Ti: $c = c_{el}T + c_{ph}T^3$

*The first reference per line is the main reference for the given value, the additional references show the range of other or similar reported values

Most reported heat capacities scaled with $K^{-1}K^{-3}$, indicating that indeed they are dominated by some phononic contribution (even if the prefactor via the Debye-model might be off). However, for SiN in particular, ref.[106] shows explicitly that if it is layered on top of a SiO substrate its heat capacity is increased substantially in the temperature range 3-10K, compared to being layered on top of substrates. The temperature-dependent

scaling was also found to be different, in this regime SiN scaled with $K^{-1}K^{-1}$. Since in our wafer stack, SiN is directly on top of SiO, I choose that specific value over the others.

A comment on the different temperature scalings K^{-n}

There exists a subtle difference between linearized and generalized units for heat capacities, which is also relevant to the application to Comsol, thus I want to comment on it:

In the vicinity of some fixed temperature T_0, the heat capacity of a material can be given in units $c = J/m^3K$, which is to be read as "J/m^3 heat capacity per unit change in temperature". This description is good as long as the heat capacity does not change appreciably around T_0. The units of c can thus be also called "linearized" [122]. For materials at room-temperature this is often indeed a good enough approximation. Elementary crystals for example reach the Dulong-Petit Limit of a constant of $c \approx 3R$ (with $R = 8.3J/molK$), which is independent of temperature [123].

At low temperatures, however, the heat capacity *does* change appreciably with each degree Kelvin, and in many cases with a T^3 dependency [79]. A linearized description around a single temperature would be wrong, and instead a more precise notation is the following : For NbN, for example, the heat capacity should be written as $c_{NbN} = \alpha_{NbN}T^3$, with $\alpha_{NbN} = 1.03\ J/m^3K^4$. For SiN, the calculation would be $c_{SiN} = \alpha_{SiN} \cdot T$ with $\alpha_{SiN} = 297J/m^3K^2$. Here, the scaling factors have generalized units J/m^3K^n, where the scaling power n reflects some details about the specific physical origin of the heat capacity.

For a scaling factor α with units K^{-n} the heat capacity is $c = \alpha \cdot T^{n-1}$. The information in table 3.1 is thus translated into Comsol by entering $c_{Comsol} = c_{here} \cdot T^{n-1}$ as the heat capacity for each material, with it's respective scaling n. This way, the overall product provided to Comsol again has linearized units J/m^3K (as required by the software), but it's numeric value now changes dynamically during the simulation. Comsol allows to put dynamic values such as T inside material parameter definitions.

As a shorthand, I still denote the heat capacities in table 3.1 with the letter c, as this is also the common usage in most published work [106], where the translation between linearized units and generalized units, the way I have spelled it out here in detail, is implied implicitly.

3.2.2 Thermal conductivities

Thermal conductivity κ is measured in units W/mK, and specifies how well heat can propagate between to points with temperature gradient $\Delta T = T_2 - T_1$ within a material. The explored literature data on experimentally measured thermal conductivities revealed a great variety of scaling powers: Constant values for SiO, linear T-scaling for Pd and Ti, quadratic T-scaling for SiN and bulk-$LiNbO_3$, and cubic T-scaling for NbN and thin-film $LiNbO_3$. For SiO in particular, the literature mentioned multiple times a "universal plateau" of constant conductivity in the range of 2-10K, which is accredited to it's amorphous structure [114].

The different temperature scalings are applied to Comsol the same way as describe above for heat capacities: For every κ given here with units K^{-n} I entered κT^{n-1} as the thermal conductance into Comsol.

Table 3.2: Thermal conductivities

Material	Thermal conductivity κ	Range	References*
SiN	8×10^{-3} W/mK^3	3-20 K	[106], [124] [109] [125] [126]
NbN	3.4×10^{-5} W/mK^4	2-10 K	[79], [127], [23]
SiO	8×10^{-2} W/mK	3-10 K	[114], [106] [114] [128] [129] [116] [117]
SiO (t.f.)	1.1×10^{-4} W/mK^3	2-10 K	[130]
$LiNbO_3$	1.5 W/mK^3	5-10 K	[131]
$LiNbO_3$ (t.f.)	3.3×10^{-3} W/mK^4	2-10 K	[118] +Casimir approx
Pd (t.f.)	3.0×10^{-1} W/mK^2	1-30 K	Via Eq. 3.3, [132] [133]
Ti (t.f.)	3.2×10^{-2} W/mK^2	3-16 K	Via Eq. 3.3, [79]

t.f = thin film

*The first reference per line is the main reference for the given value,
the additional references show the range of other or similar reported values

Thin layers

In very thin materials, phonons can experience additional scattering losses at the boundaries compared to bulk materials. This influence becomes significant when the thinnest dimension of the material is comparable or smaller than the mean free path of the phonons [134]. In this regime, one can make the approximation that the new mean free path of the phonons is just given by the geometric limitation, and calculate the thermal conductance via the Casimir-Limited approximation [135][134]:

$$\kappa = \tfrac{1}{3}\, v\, c\, l \tag{3.2}$$

where v is the averaged sound velocity in the material, c is the heat capacity and l is the film thickness. As one example, the mean free path of phonons in SiO at T=2K is λ =500nm [106]. Any layer thinner than 500nm would thus have reduced thermal conductivity compared to published bulk values.

I follow the approach in [136] and use this Casimir-limited approximation to calculate the thermal conductivity for the 330nm thin $LiNbO_3$ layer, using for the bulk heat capacity the value reported in table 3.1 and as sound velocity the value v =7km/s [?].

The only other thermal conductivity of $LiNbO_3$ I could find was given for a bulk crystal and is reported in [131]. Comparing these two values, the Casimir-Limited approximation gives a value by a factor 50 smaller than the bulk value for the temperature Since this is a rather big discrepency, this would be one of the most relevant material parameters to check in again.

Wiedemann-Franz Law

For metals with known resistivity ρ the Wiedemann-Franz law [132] can be used to calculate the thermal conductance:

$$\kappa = L_0 T/\rho \tag{3.3}$$

where $L_0 = 2.44 \cdot 10^{-8}\mathrm{V}^2\mathrm{K}^{-2}$ is the Lorentz-constant. I use this law to calculate the thermal conductivities of Ti and Pd because I have access to their resistivity values for very thin films at cryogenic temperatures (see section 3.2.4) which fits quite well to our desired simulaition situation.

3.2.3 Thermal boundary conductances

Thermal boundary conductance G is measured in units $\mathrm{W/m^2K}$ and specifies how well heat can propagate between the interface of two materials with a temperature gradient of $\Delta T = T_2 - T_1$. By units, it can be distinguished from thermal conductances due to it's m^-2 scaling instead of m^-1. The physical origin of the boundary conductance lies in a mismatch between the phononic modes of two touching materials [137]. The less similar the respective phononic modes are, the higher the probability that a phonon incident on the boundary will be reflected instead of transmitted. This results in a lower heat conductivity through the boundary.

One way to model the phononic mismatch between two materials is given by the Diffusive mismatch model (DMM) [138]. I follow here closely the treatment by Dane et al. [135] from Berggrens Group, since their work is directly concerned with modeling SNSPDs and similar thin film superconducting devices at cryogenic temperatures, providing an excellent fit for our desired application. Further details on the thermal modeling of specifically NbN and similar materials can also found in the thesis by Dane [122].

Given two materials, their thermal boundary conductance in the DMM model can be expressed via the Kapitzka cooling rate Σ_K [139], which is given by

$$\Sigma_K = \frac{\pi^2 k_B^4}{120\hbar^3} \cdot \frac{[1/v_{1L}^2 + 2/v_{1T}^2] \cdot [1/v_{2L}^2 + 2/v_{2T}^2]}{[1/v_{1L}^2 + 2/v_{1T}^2 + 1/v_{2L}^2 + 2/v_{2T}^2]} \tag{3.4}$$

where v_{iL} and v_{iT} are the longitudinal and transversal speed of sounds of the two materials.

If two interfacing materials have different temperatures T_1 and T_2, the heat transfer P_{12} from the hot to the cold material can then be calculated via the black-body phonon assumption [122] [135] via

$$\frac{P_{12}}{A} = \Sigma_K \left(T_1^4 - T_2^4\right) \tag{3.5}$$

where A is the contact area between the materials. For small temperature-differences ΔT, the black body scaling can be linearized around a single temperature [136]. Note that an extra factor 4 appears due to this linearization.

$$\left(T_1^4 - T_2^4\right) \approx 4T^3 \Delta T \tag{3.6}$$

The heat transfer can then also be expressed in this linearized form

$$\frac{P_{12}}{A} \approx 4\Sigma_K T^3 \left(T_1 - T_2\right) \tag{3.7}$$

Now for comparison, in Comsol heat transfer between boundaries is treated with the following equation

$$\frac{P_{12}}{A} = h_{12}(T_1 - T_2) \tag{3.8}$$

We see that to translate between the Kapitzka-Model and Comsol, one needs to do the following identification:

$$\Rightarrow h_{COMSOL} = G_{12}T^3 = 4\Sigma_K T^3 \tag{3.9}$$

where I introduced the intermediate notation $G_{12} = 4\Sigma_K$, following [79] and [139]. When combining values from literature, one needs to take there of whether, and where, this prefactor of 4 might be hidden.

I use the Kapitzka-Equation 3.4 and sound velocities from [136] to calculate the thermal boundary conductance parameter Σ_K for every pairwise combination of our materials of interest (excluding NbN, see next paragraph), multiply by four to translate into the format $G_{12} = 4\Sigma_K$, and report these values in table 3.3. Note that again, I enter the values into Comsol as $G_{12}T^3$ to have correct units and correct temperature scaling.

Thermal boundary values for NbN I took as Σ_K directly from [135], marked in bold font in table 3.3, since those were calculated with the more involved acoustic mismatch model (AMM) and reported to match even better with experiments. For the rest of the pairs I had to resort to own calculations. A full overview on the topic of thermal boundary conductance can be found in [137], a more modern review in [138]. Experimentally, its has also been tried to extract cryogenic thermal boundary parameters using superconducting nanowires as thermals sensors [140].

Table 3.3: Thermal Boundary Conductances. Normal font: Calculated via eq. 3.4. Bold font: Retrieved from [136]. Mind the factor 4 in the definition of G_{12} (eq. 3.9)

G_{12} [W/m^{2}K^4]	Si	SiO	SiN	$LiNbO_3$	NbN
Si	-	-	-	-	-
SiO	538	-	-	-	-
SiN	359	441	-	-	-
$LiNbO_3$	559	785	455	-	-
NbN	**532**	**656**	**484**	**824**	-
Ti	624	917	496	981	694

3.2.4 Thin film electrical resistivities

The electrical resistivities ρ of materials are remeasured in Ω m and specify the electrical resistance per square. To translate them to resistances R_{sq}, one has to divide by the thickness d of the material:

$$R_{sq} = \frac{\rho}{d} \tag{3.10}$$

Very thin films of metals can have substantial amounts of resistance compared to the same metal in bulk [141] [142]. One reason is increased sidewall and surface scattering at small scales. Since the envisioned resistors in our thermal switch will be rather thin, I tried to find measurements of the thinnest possible films. The best I could find were measurements of ca. 30nm thin films, their resistivities are reported in table 3.4. Given the increasing resistivity for thinner and thinner films in [141], films even thinner than 30nm might have higher resistivities than those reported here. For NbN, I take an average of multiple reported thin-film normal state resistivities as detailed in section 2.1.5

Table 3.4: Electrical Thin-Film Resistivities at 2K

Material	Electrical Resistivity ρ @ film thickness	Reference
Au	10 Ω·nm (@ 35 nm)	[142],[141]
Pd	80 Ω·nm (@ 26 nm)	[141]
Ti	750 Ω·nm (@ 30 nm)	[135]
NbN	2500 Ω·nm (@ 5nm)	[25] [49]

3.3 Geometry and Boundary Conditions

Two natural designs arise for the placement of the heating element relative to the superconductor: Next to the superconductor, or on top of it. Both configurations are shown in Fig.. 3.3, I will call them sideheater and topheater, respectively. The sideheater would be easier to fabricate since it doesn't involve stacked layers, while the topheater is expected to have a stronger heat coupling due to the close distance between heating resistor and superconductor.

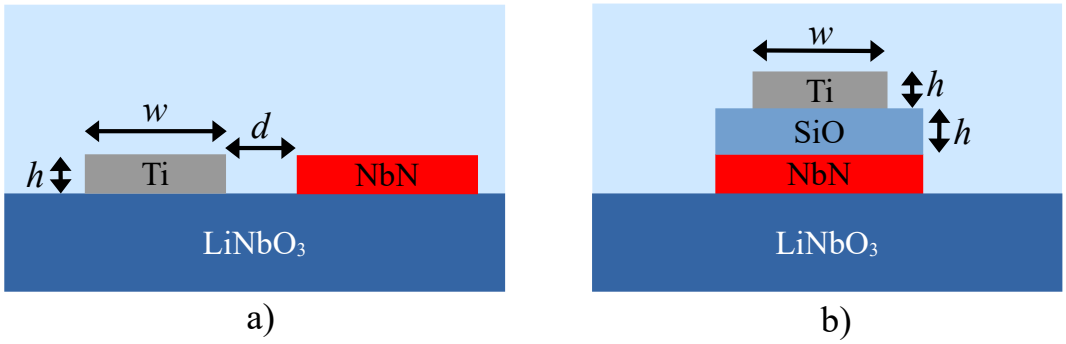

Figure 3.3: Sketch of the two investigated heating geometries: sideheater (a) and topheater (b).

The marked dimensions in figure 3.3 denote the most relevant fabrication limitations: To have enough uniformity in height, the deposited metal should be at at least 3nm thick.

To not have the metal layer stripped off from the chip during liftoff, the width should be at least 400nm and the clearance to the nearby superconducting strip at least 200nm. For the topheater, the dielectric buffer layer must be at least as thick as the superconducting strip (5nm) to cover it also over the edges.

For the heating resistor, I chose as the simulated dimensions directly the limitations given by fabrication, to get an upper limit on a possible performance. I.e., the heating resistor is as narrow and thin as possible to provide highest resistance per area leading to strongest heating per area. As the initial resistive material I chose Titanium, as it had the highest resistance of the available metals in our selection.

For the buffer layer, I chose 10nm SiO, following some typical similar designs in literature (section 2.2). For the nanowire, I chose the default 5nm film thickness, and a width of 400nm for the Sidehater and 750nm for the topheater. An overview off all geometric values used for simulation is given in table 3.5.

Table 3.5: Dimensions used for the thermal simulations.

	sideheater	topheater
h_{Ti}	3 nm	3 nm
w_{Ti}	400 nm	400 nm
d	200 nm	-
h_{SiO}	-	10 nm
w_{SiO}	-	750 nm
h_{NbN}	5 nm	5 nm
w_{NbN}	400 nm	750 nm

The substrate stack below the thermal switch is 330nm $LiNbO_3$, 3.3µm SiO and 525µm SiO, as shown in introduction 2.2. For the thermal simulation purpose, I include the full $LiNbO_3$ layer and half the SiO-Layer, but exclude any Si. I saw in initial simulations that the relevant changes in the substrate temperature are mainly in the $LiNbO_3$ near the heating element, and already within SiO the temperature barely changed.

I will do two simulations in which the setup is further slightly changed from the by now described design. These cover two common cases encountered in fabrication: Cladding, which is usually applied for mechanical protection, and SiN, which is the most popular waveguide material for general photonic applications.

With Cladding: In one simulation, I will try different heights of an additional cladding layer on top of the chip. Cladding is a protective layer often added at the end of chip fabrication. It's material is a type of glass, so I will treat it in simulation as SiO. We will compare four different cladding heights $h_{cladd} = \{$0nm, 100nm, 300nm 1000nm$\}$. Usually the precise cladding height is not relevant for it's purpose, but here I expect that the thermal situation could differ between e.g. 100nm and 1000nm cladding, and especially between some cladding and no cladding.

SiN as waveguide: In a second simulation, I use SiN instead of $LiNbO_3$ as the waveguide substrate. Even though for our proposed chip the waveguide material would need to

be $LiNbO_3$, it is interesting to see how the thermal situation compares for SiN.

I choose to simulate the thermal switches in 2D, i.e. simulate only a crossection along the strip lines. This is because in a real design, I expect the heater to be relatively long compared to it's width, such that a large resistance (multiple kΩ at least) could be created by the NbN switching into the resistive state. In such a long heater, every crossection, especially in the center of the heater, would not notice the spatial extend along the length. Using a 2D simulation allowed much faster simulation times, giving more flexibility in different parameter sweeps and faster feedback.

Boundary Conditions

I set 2 K as the initial temperature for all materials, as this is the experimental condition. I also use $T = 2$K as the boundary condition for the bottom and side surface of the SiO-Layer. Above the thermal switch there is no material. The cryostat used for our experiments works under vacuum, in absence of exchange gas. There is thus no convective cooling at the upper surface of the chip. Thermal radiative cooling can be completely neglected at cryogenic temperatures.

Applying a Heating Pulse

I want to apply a heating pulse to the resistive layer to observe in simulation how much the temperature of the superconducting layer below is influenced. Additionally, I want to know the time scales of this interaction.

To this end, we define a rectangle heating pulse $I_{ht}(t)$ that is active between $t = 0$ and $t = 50$ns, during which window it delivers a constant heating current I_{ht} through the metal resistor. For the magnitude of the heating current I choose to simulate three values: $I_{ht} \in \{10\mu A, 33\mu A, 100\mu A\}$. These lowest value is oriented at a typical bias current from an SNSPDs, while the larger ones are for comparison to probe higher currents. I simulate a duration of 100ns, such that during the first half of the simulation the heater is active while during the second part it is off, allowing us to see the cooldown dynamics. The choosen time step resolution is 0.1ns.

3.4 Results

I simulated four different setups: A sideheater, a topheater, a topheater with added cladding, and a topheater with SiN instead of LiNb3 as the waveguide material.

The the main point of interest in the results is the temperature of the NbN. For use as a switch, the temperature of the NbN would need to reach it's critical temperature T_c, i.e. around $T = 8$-10K or beyond.

Sideheater

The first simulation was done for the sideheater design. A view of the temperature distribution around the heater is shown in figure 3.4. It is given at the timestamp just before the heating pulse of is turned off (at t=50ns) and for the case of strongest heating, I_{ht}=100µA. For better visibility of the thin layers, the view is stretched by factor 4 in the y-direction. Temperature-curves taken at the centers of both the heater and the NbN are given in figure 3.5.

The heat remains for the most part directly below the heater and does not propagate to the sides, i.e. also not to the NbN. The heater's temperature increases appreciably, to around 5K, 8K and 15K, respectively for the three heating current of 10µA, 33µA and 100µA, respectively. That is, even with the lower current of 10µA the temperature is locally raised by multiple degrees.

However, non of this heat reaches the NbN. During the simulation period, it's temperature only increases from 2.00K to around 2.04K, close to zero change. There is additionally a time delay of several 10's of ns for the heat propagation between the heater and the NbN.

Topheater

The second simulation was of the topheater design. A view of the temperature distribution around the heater at t=50ns is shown in figure 3.6 and the temperature-curves are given in figure 3.7.

In this topheater design, the NbN temperature increases appreciably. After ca. 1ns after the heater is turned on, the NbN's temperature rises to ca. 6K, 10K and 18K, respectively for heating currents 10µA, 33µA and 100µA. The critical temperature regime of T=8-10K is thus reached for Ih=33µA, while it is considerably surpassed for Ih=100µA.

The NbN quickly (1ns delay to the heater) reaches a plateau in temperature, which does not change appreciabely for the next 49ns of the heating pulse, indicating a thermal steady state that is quickly reached.

After the heater is turned off, the cooldown of the NbN happens in two distinct phases. Within 1ns, temperature drops from the steady state plateau to some lower intermediate plateau temperature. This initial drop happens on the timescale of 1n. Then, from there on, the temperature decreases much more slowly with time, thermalizing on the order of µs' to the background temperature of 2K. The initial fast drop from the steady state plateau to the intermediate plateau is from 6K to 2K, from 10K to 4K, or from 18K to 6K, respectively for the three heating current.

The drop from 10K to 4K of the NbN is particularly interesting: The temperature changes from the normal state regime to well within the superconducting regime within ca. 1ns. This means that the NbN would become superconductive right after the heating is turned off. The time scale of this thermal cooldown is even shorter than for example some electrical SNSPD timescals, as for example the typical detection reset time of order 10ns.

The 100µA heating current might be so strong that it degrades the performance of the switch again. Once NbN is resistive (beyond Tc =8-10K), further heating does not

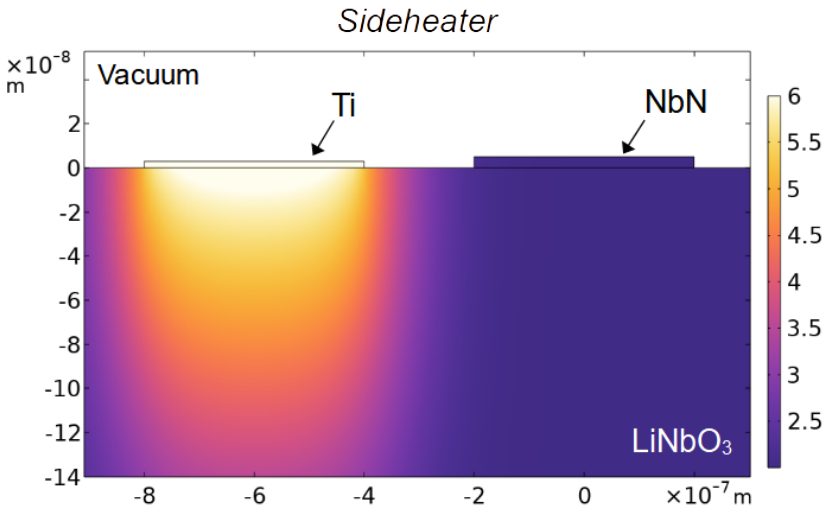

Figure 3.4: Snapshot of the sideheater-configuration at the end of the heating pulse (I_{ht} =100µA). The Y-Axis is stretched by a factor of four for better visibility. The NbN remains completely cold.

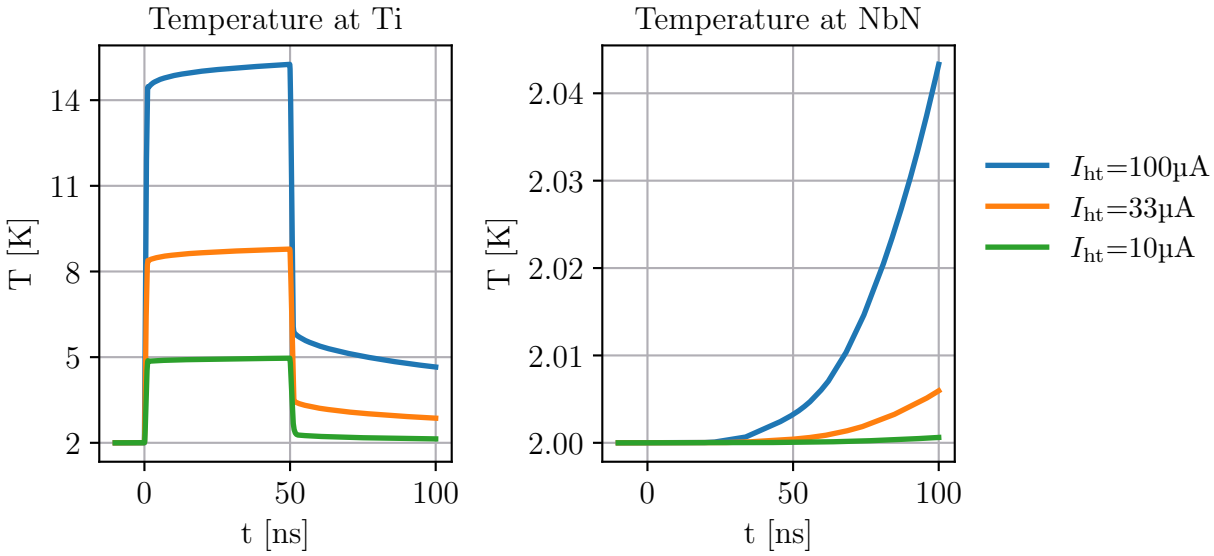

Figure 3.5: Temperature-curves of the Ti- and NbN-Films in the sideheater design, taken at the centers of each respective film

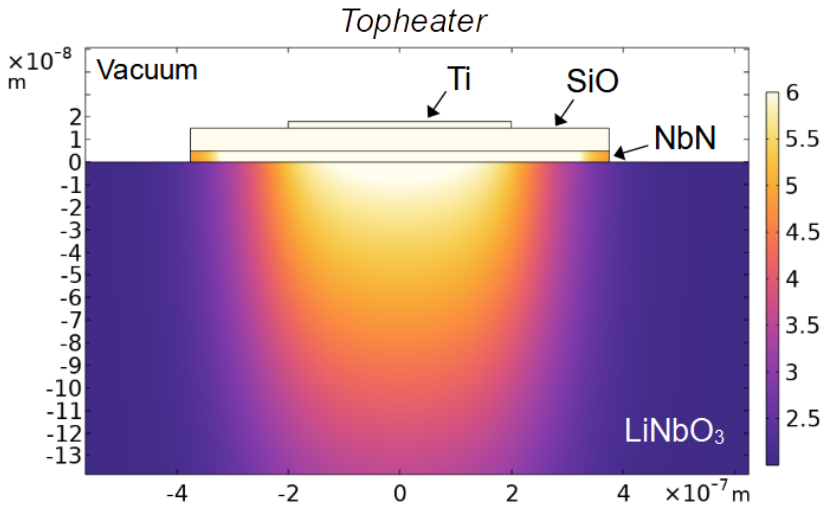

Figure 3.6: Temperature-distribution of the topheater at the end of the heating pulse (t=50ns) for I_{ht} =100µA. The Y-Axis is stretched by factor 4 for better visibility.

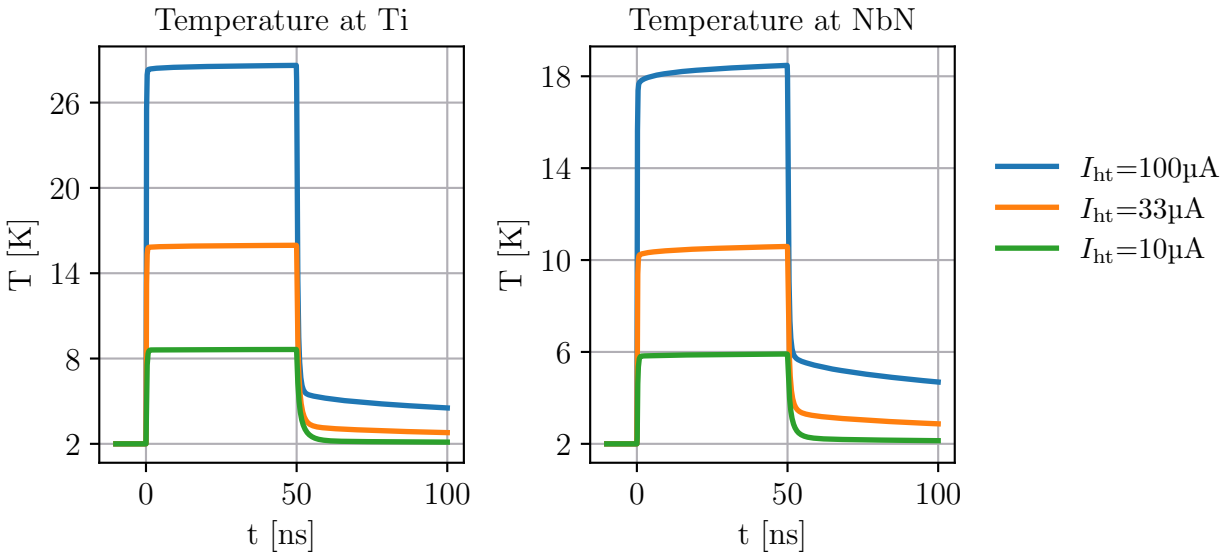

Figure 3.7: Temperature-Curves of the Ti- and NbN-Films in the topheater design, taken at the centers of each respective film

change its electrical properties. However, it increased the temperature after the initial drop, whic via the Ginzburg-Landau-Relation Ic(T) reduces the critical current the NbN could support right after its initial cooldown.

Cladding

The third simulation included a topheater with additional cladding, with thicknesses ranging from 0nm to 1000nm. An complete overview of the simulated domain is given in figure 3.8, which includes a zoomed view around the topheater region. The temperature curves are reported in figure 3.9. The maximum heating current of 100µA was choosen for this comparison.

Two things can be spotted: The presence of the cladding has a significant impact on the temperature of the NbN, while the exact thickness of the cladding as almost no impact.

Without cladding, the NbN reaches a temperature 18K (same as in the simulation before). With cladding, this temperature is reduced to 8K, a cooling effect of ten degrees. Also visually one can see that the cladding offers the heat a new pathway to propagate away from the heater (upwards into the cladding), reducing the heat that propagates downwards into the NbN.

Changing the cladding height from 100nm to 1000nm changes the plateau temperature of the NbN by only half a degree. The exact thickness of the cladding has thus barely an influence on the NbN's plateau temperature.

For the cooldown dynamics, the thinnest cladding layer (100nm) leads to slower cooldown than thicker layers (300nm, 1000nm). This might be because in the thinnest layer, the heat does not have as much space to propagate away once the heater is turned off.

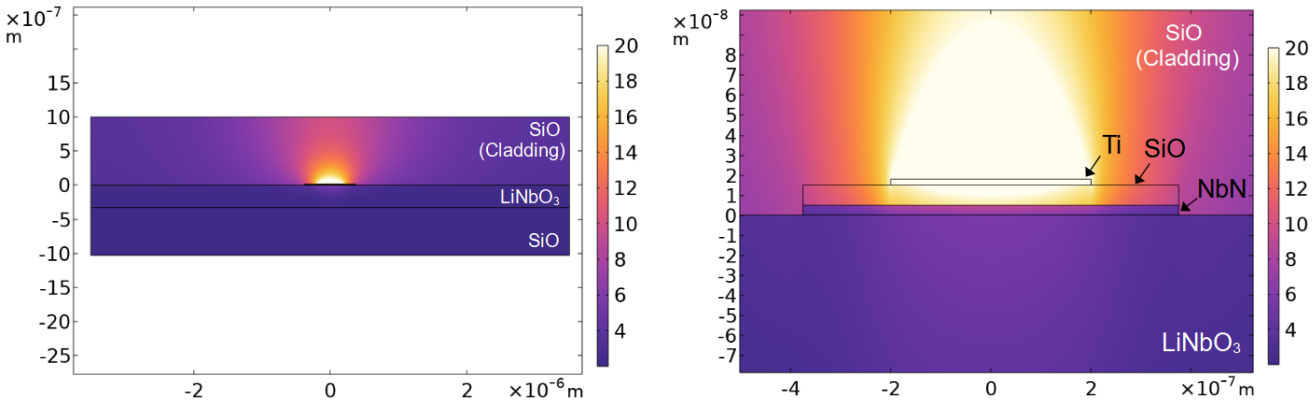

Figure 3.8: Temperature distribution after t=50ns for a topheater with 1000nm Cladding added (for Iht=100µA). Full view (left) and zoomed view (right)

SiN as waveguide material

Finally, we compare the waveguide materials $LiNbO_3$ and SiN. I use the topheater design and a heating current of 33µA for the comparison. The temperature-curve of the NbN for the different waveguide materials below it is given in figure 3.10.

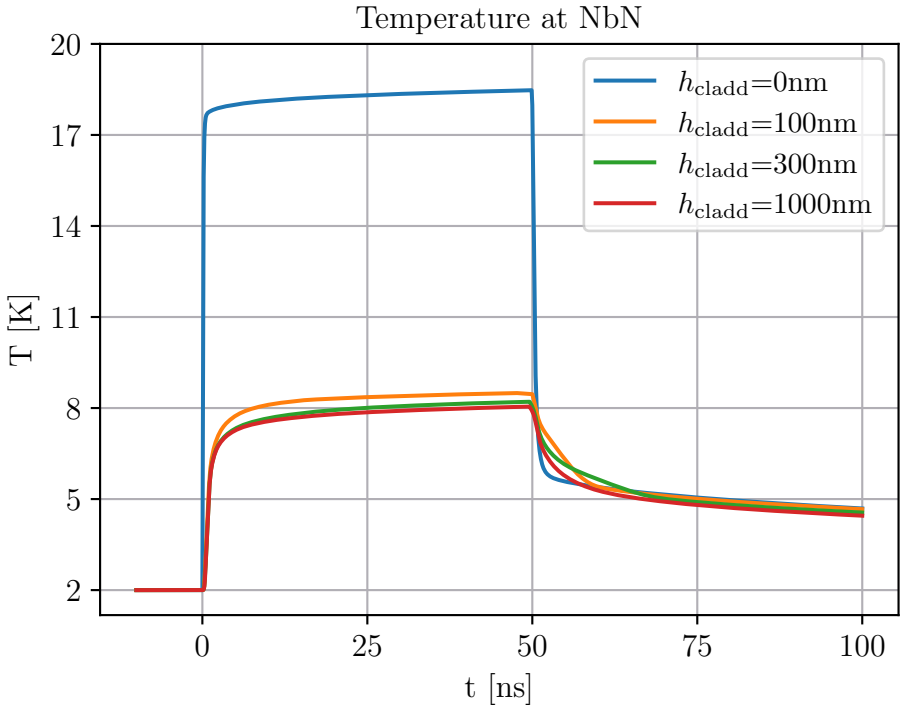

Figure 3.9: Temperature-curves for a topheater with added cladding heights, with Ih=100µA.

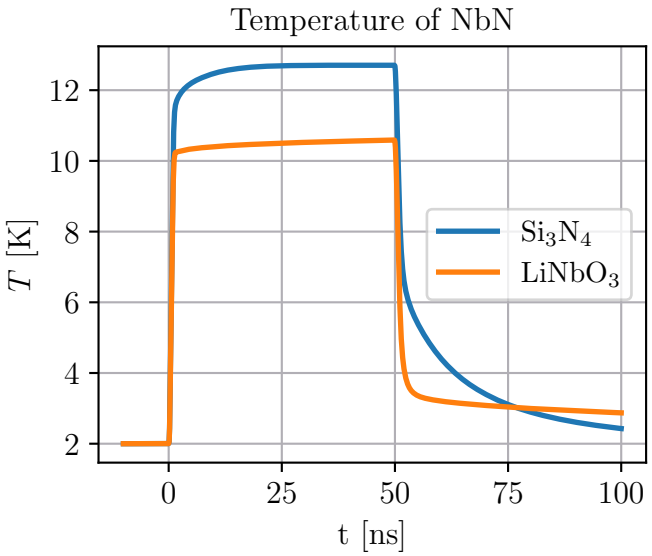

Figure 3.10: Temperature-curve of NbN, given different waveguide materials (SiN or $LiNbO_3$). The Setup is a topheater with Ih=33uA and no cladding.

With SiN as the waveguide material, the NbN reaches a temperature of ca. 12K, two degrees more than for the case of LiNbO. The rise time with SiN is similar to that of $LiNbO_3$, and also a for SiN a plateau temperature is quickly reached.

Whereas with $LiNbO_3$ the NbN showed a distinct two-phase cooldown, the cooldown with SiN is a single continous dropoff. The initial temperature drop is slower and less pronounced than for $LiNbO_3$, while at longer times (beyond 25ns) the provided cooldown of SiN surpasses that of $LiNbO_3$.

3.5 Conclusion of Chapter 3

On the simulation results

The topheater design allowed to heat up the NbN-film to and beyond 8-10K for heating currents in the range of 30µA, indicating the use as a thermal switch. 30µA is close enough to typical SNSPD critical currents (Ic = 10-20µA) that such a thermal switch might be integrated together with SNSPDs in a single circuit, and that the SNSPDs could even control the heating current.

The magnitude of the heating current however should also not to be too high, as otherwise it slows down the cooldown of the switch and reduce the supported critical current. For our design, 100µA was so strong that it limited the initial temperature drop of the NbN down to 6K, while Ih=33µA allowed an initial drop down to 4K, which increased the dynamic range between resistive and superconducting state.

The sideheater did not show any promising results as a thermal switch. The NbN remained almost completely cold, with it's temperature only increasing from 2.00K to 2.04K during the simulated 100ns.

Cladding significantly reduces the maximum temperature of the NbN (from 18K to 8K in the given example) because it is a heat sink directly in contact with the heater. In chips where cladding is required, this leads to higher required heating currents (on the order of 100-200µA) to still achieve a resistive state in NbN compared to no cladding. The exact thickness of the cladding has negligible thermal influences in comparison.

$LiNbO_3$ as a waveguide material led to a distinc two-phase cooldown, with a rapid initial drop in temperature and a slower thermalization afterwards. The large temperature contrast of the rapid initial drop seems promising for the use as thermal switches with fast response times on the order of few ns. In comparison, SiN led to a single continouous cooldown, with a lower initial cooling rate.

On the collection of the thermal parameters

Finding robust thermal parameters for cryogenic temperatures proved to be more difficult than initially anticipated. Due to exotic new physical excitations and phenomena at low

temperatures, theretical predictions and models are much more involved than standard approaches, and beyond the scope of this thesis. I relied instead mainly on experimentally measured data, where the unknown precise physical interactions would be contained at least in an effective sense in the reported parameters.

Besides the cryogenic requirement, also the thin film modelling required additional attention. For thin films, thermal conductances are reduced compared to bulk sizes due to increased scattering losses at the boundaries. I used the e.g. the Casimir-Approximation and the Wiedemann-Franz Law to find thermal conductivities for thin films, but the decision of from which point on a material should be treated as a thin film is not always obvious. Physically, the relevant size scale is given by the mean free path of the phonons, but this information is not always available, especially for cryogenic temperatures.

The topic of thermal boundary conductance proved to be somewhat simpler to handle because the DMM-Model provided a direct formula to calculate the boundary conductance between any two given materials. It was lucky to have Dane et al. [135] which presented a thorough treatment, and the option to find further details in the corresponding thesis [122].

Chapter 4

Investigating new superconducting readout-circuits

In this chapter I develop and investigate three new electrical circuits that could interface between an SNSPD and a LiNbO-EOM for optical readout.

To this end, I first discuss the figure of merit and give an estimate of the required value, then present the simulation software employed in this chapter. The three proposed circuits are then discussed in their order of complexity. All three fulfill the key requirement that the SNSPD resets into it's superconducting state after a photon detection. Achieving this resetting-property while still optimizing for highest circuit-performance was one of the main challenges.

The third circuit incorporates a thermal switch, for which I discuss how I adapted the simulation technique to treat such an electro-thermally coupled system.

Figure of merit

The central figure of merit of the circuits is the voltage V_{out} across the EOM. It determines how strong the signal from the SNSPD is transceived into the optical domain and thus available for optical readout.

Previously published work allows to do a rough estimate of a sufficient magnitude of V_{out}: In the work by de Cea et al., the SNSPD provided a signal of 2mV and the EOM had a modulation efficiency of 700pm/V, which in combination led to a resonance shift of 1.4pm, sufficient for optical readout (see introduction 2.3.2).

In my setup, with a LiNbO3-Racetrack EOM, the reported modulation efficiencies on the order of 3-8 pm/V (see introduction 2.3.2). If I are conservative and take 3 pm/V as the modulation efficiency, then to achieve a similar resonance shift of 1.4pm the voltage signal V_{out} would need to be around 460 mV.

Since an SNSPD only delivers a voltage of ca. 1mV (in a default circuit), the to-be-designed circuits needs to provide by some means a voltage ca. two orders of magnitude larger to be applicable to optical readout.

A second parameter of merit is the detection reset time for each circuit, which we denominate with Δt_{90} and is defined as the time it takes after a photon absorption until the SNSPD returns to 90 percent of it's initial bias current, because at this point the

original detection efficiency of the SNSPD is mostly recovered. Higher output voltages are generally linked to higher reset times, leading to some trade-off. I report a range of parameter combinations for each circuit which show the extend of this trade-off.

4.1 Simulation tool

LTspice

We use LTspice to simulate the electrical circuits under investigation. I use the LTspice model for SNSPDs developed by Berggren [57], which allows to generate SNSPDs within LTspice and interface them with other circuit components.

The SNSPD-component developed by Berggrens group approximates the electronic behaviour of SNSPDs, within the constraints of the LTspice environment. Photon absorption is modelled as a sudden small increases in the current through the SNSPDs. The component also includes dynamics for e.g. the thermal heat dissipation and the dynamic hotspot size. A screenshot of the module in LTspice and an overview of some available settings is shown in figure 4.1.

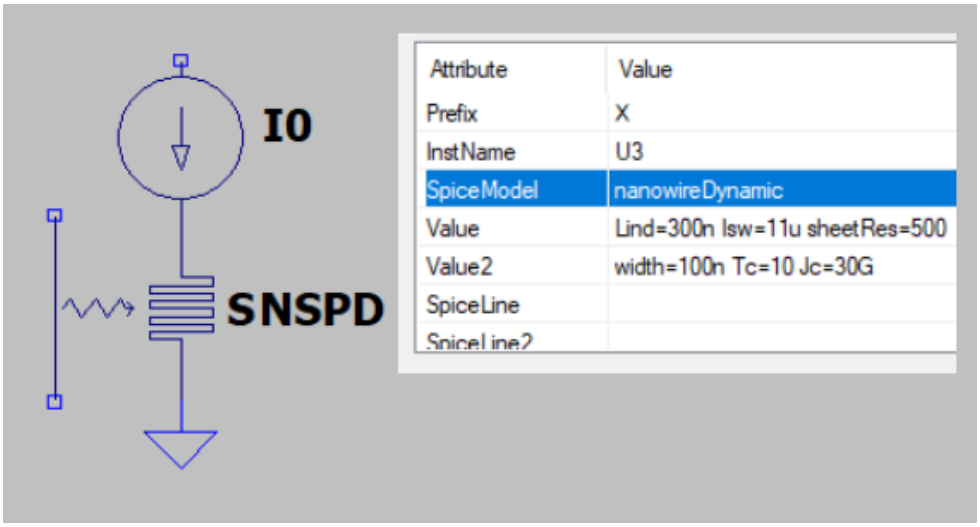

Figure 4.1: The SNSPD-Module in LTspice with customization settings

The exact customized parameters that I used for every SNSPD in this chapter are given in table 4.1.

One parameter that I did not change was the thermal boundary conductance parameter to the substrate, which is the default value chosen by the developers to model thermal contact with sapphire, as sapphire is one of the substrates with the highest thermal boundary conductance with NbN [136]. As I have seen that this value does have effects, e.g. on I_h, for future simulations it would be useful to adapt this thermal boundary conductance also manually (in the configuration files; one can not set it via the customization window) to better match the specific substrate of interest. The new parameter could be chosen

Table 4.1: The customized parameters used for the SNSPD-Module in LTspice in this thesis.

Lind	300n [H]
Isw	11µ [A]
sheetRes	500 [R/sq]
width	100n [m]
Tc	10 [K]
Jc	30 [GA/m^2]

e.g. from table 3.3, keeping it mind that it would need to be linearized around some temperature because the SNSPD module only works with linearized units W/m^2K.

Modelling the Racetrack-Modulator

Since LTspice is an electrical circuit simulation software, we need to represent the electro-optical Racetrack-Modulator in this environment. In most designs it consists of two electrodes between which a voltage is applied (compare e.g. figure 2.11). This is most similar to a Capacitor, thus I model the Racetrack-Modulator as a Capacitor with capacitance C_{EOM}.

To determine a realistic capacitance, I searched the literature for similar setups. Reported values for such electrode geometries are 100pF/m [143], 180pF/m [144] and 200pF/m [145], from which I settle on an average of 175pF/m. The racetrack-resonator on which I based the modulation efficiency estimates on which is most similar to our fabrication process was ca. 400µm long [102]. I use this value for a typical length of 400µm, which results in $C_{EOM} = 70$fF.

Using Meanders as Inductors

The relatively high inductance of superconducting films ($L_{sq} \approx 0.1 - 0.5$nH/sq) can be used to built integrated inductors [146]. By arranging e.g. a NbN-strip of length 1.000 squares into a compact meander geometry (as shown e.g. in figure 4.2), an inductance of ca. 0.5µH can be achieved.

If compared to other typical integrated devices, the footprint of such a meander can be quite large. For an inductor with a desired inductance L and a maximum current I that should be supported, it's footprint area A can be estimated via

$$A = \frac{L}{L_{kin}} \cdot 3 \cdot w(3I)^2 \tag{4.1}$$

where L/L_{kin} is the number of inductive squares and $w(3I)$ the width of the nanowire strip as a function of I, e.g. using equation 2.7. Each square has then area w^2. Because strip-lines can not be fabricated directly next to each other, there is some gap between

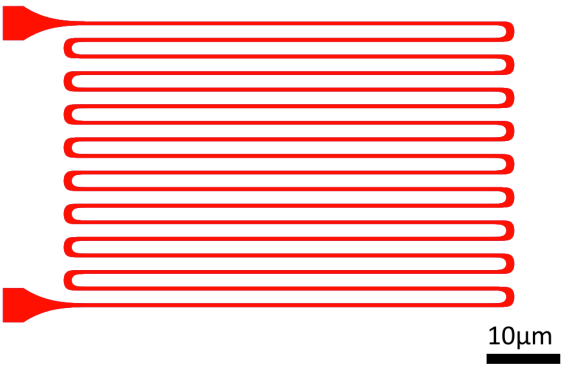

Figure 4.2: Design of a superconductive meander for use as an inductor

them, typically a distance of ca. $2w$, thus each square in the meander takes up an effective footprint of ca. $3w^2$.

To take into account that local constrictions due to fabrication imperfections can happen along the long meander, I dimension the nanowire width not such that it exactly supports $I_c = I$, but instead make it wider by a factor three, i.e. a safety factor, to have a margin of $I_c = 3I$.

One example: A meander with Inductance 50µH and supporting current up to 60µA is desired. This would result in $N = 100.000$ squares and a needed safety width of $w = 1.1$µm, giving a total footprint of 607 x 607 µm^2. This limits high density integration.

For all the following circuits, the inductors are meant to be fabricated via such longer superconducting meander as presented here.

4.2 Heuristics that guided circuit design

Here, I want to give a brief comment on some of the train of thoughts that motivated the design of the upcoming circuits:

Charging the EOM

The voltage V_{out} across the EOM can also be expressed as $V_{out} = Q/C_{EOM}$, where Q is the total charge accumulated at the EOM. To maximize the voltage, one can thus also equivalently think about maximizing the charge accumulation Q at the capacitor. Now, the circuit is continuously sourced with charges, via the constant current source I_0. These charges must go somewhere, they cannot disappear.

If one now wants to direct as many of these charges into the EOM, increase it's charging Q, the other pathways for the current to reach ground should have a resistance (or for transient events, impedance) as high as possible. Since C_{EOM} is fixed and Q is dependent on the rest of the circuit, this now motivates the question whether the impedance of the other circuit elements can be significantly increased.

Driving the SNSPD into high resistance

According to the hotspot growth model (see introduction 2.1.8), the resistive domain within an SNSPDs could in theory grow to almost arbitrarily large sizes (until the whole nanowire is resistive), as long as enough current is flowing to supply the joule heating expansion.

In typical interfacing circuits, this theoretical possibility is almost never explored because the bias current is quickly (in less than 1ns) redirected away from the SNSPD, stopping the expansion of the resistive domain at around 1-2kΩ. However, nothing stops this resistive domain to grow much larger, if only the current is supplied.

With a typical growth speed of 5 kΩ/ns, with continued biasing a SNSPD could reach a resistance of e.g. 50kΩ within just 10ns. Such a higher resistance would be exactly what would be needed according to the prior considerations about EOM charge accumulation.

Inductor as the Current-Controller

Now, it is of course possible to design a circuit that just keeps forcing current into an SNSPD until it is completely resistive (which would be on the order of 1MΩ). But this would not be helpful as then the SNSPD would never return to it's superconducting state, and would never be able to detect a next photon.

The circuit should be designed such that only at some *initial time*, say in the first 5-10ns, the current is forced through the SNSPD to increase it's resistance, while then at some *later times* there must open up some alternative low-impedance sink for the current to redirect to. The redirection must be such that the remaining current through the SNSPD falls below it's hysteresis current value I_h.

This is now where an additional Inductor, in parallel to the SNSPD and the EOM, seems promising. Due to it's intrinsic inertia against sudden current changes, it could fulfill what is required for SNSPD biasing: At initial times, the inductor prevents any current entering due to it's high inertia, forcing the current to continue to flow through the SNSPD (and into the EOM as well). At later times, however, especially as by then the SNSPD will have appreciable resistance, the inertia of the inductor is overcome and more and more current through it will have build up. If this current redirection is large enough such that the current through the SNSPD fall below I_h, it could reset back into superconductivity.

At this point, since now the resistance of the SNSPD is again zero, the biasing current would after some time return into it and the detection cycle would be complete.

4.3 Circuit 1: Voltage amplification via a highly-resistive SNSPD

The first proposed circuit, following the considerations above, I add an Inductor L_1 in parallel to the SNSPD. The circuit is shown in figure 4.3, with the corresponding LTspice simulation next in figure 4.4. The source current is $I_0 = 10\mu A$ while the critical current

of the SNSPD is $I_c = 11\mu A$ (as for all SNSPDs in this chapter). This means the SNSPD is biased at 91%.

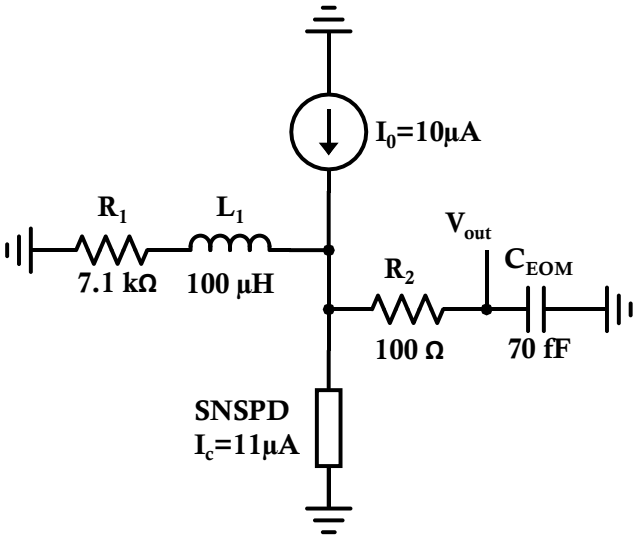

Figure 4.3: Circuit 1

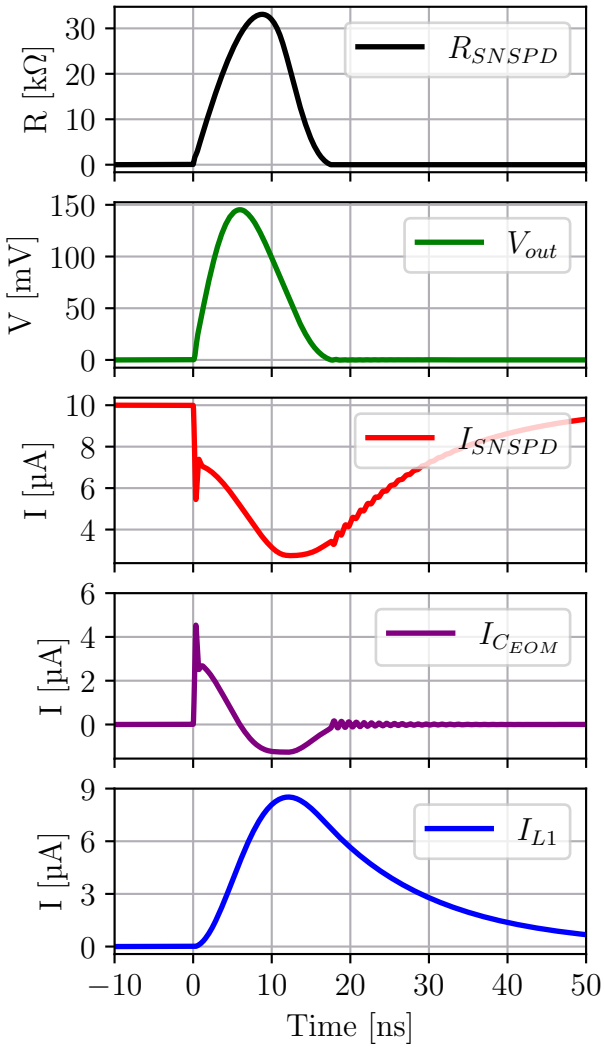

Figure 4.4: LTspice simulation of Circuit 1

Comment on the Resistors

There are two ancillary resistors in Circuit 1. Resistor R_1 is in series to the inductor and forces the current back into the SNSPD once it is superconductive again. The characteristic time of this return current is $\tau_{ret} = L_1/R_1$. To optimize for fast count rates it should be as small as possible. However, if it is too small, latching occurs. Meaning that for every inductor value L_1 there exists an best choice that provides the fastest current return while still giving the SNSPD enough time to reset into superconductivity beforehand. In table 4.2 a list of such optimal parameter pairs is given, with the corresponding performance metrics of the circuit.

In the presented circuit 1 I chose $L_1 = 100\mu H$, which gave rise to an optimal resistance value of $R_{1,max} = 7.1k\Omega$. It is to note that no latching occurs even though R_1 is much larger than the impedance of $Z_0 = 400$ Ohm presented in the introduction of to latching (section 2.1.7). This is because here the equally larger inductor L_1 is relevant for the return time and no longer the much smaller kinetic inductance L_{kin} of the SNSPD.

Resistor R_2 in series with the Capacitor had to be added to damp oscillations between L_1 and C_{EOM}. The value is not as relevant, as long at it is large enough to damp the oscillations and small enough to not disturb the other circuit dynamics. I found that 100 Ω sufficed. In the curves in figure 4.4 on can still spot small remnants of this oscillation.

SNSPD Resistance

The simulation now gives concrete insight into the resistance of the SNSPD, plotted in figure 4.4. It's peak resistance is R=33kΩ, reached after 8ns. This gives an average resistance growth rate of 3.8kΩ/ns, similar to the manually calculated order of magnitude of 5kΩ/ns.

Charging the Capacitor

The current entering into the Capacitor is on the order of 2µA during the first ca. 3 ns after the SNSPD click. This means that the Capacitor absorbs ca. 20% of the total overall source current and stores it as charge, not a small fraction. The EOM itself could thus potentially be also beneficial as a temporary sink for current redirection. That transient charge accumulation near to an SNSPD can affect it's operation has also been discussed in literature, see e.g. [147] [148] [149].

Inductor as a Sink

The inductor works as expected, it resists initial current builup while still providing at some point the main sink for the current. At ca. 12ns, the current through the inductor reaches it's peak value of close to 9µA. At that point thus 90% of the source current is redirected into the sink path. Note that the current through the SNSPD at that point is not 1µA but a bit higher, because of some released charge by the capacitor.

The value of the inductor can be choosen in a wide range. I report in table 4.2 results ranging from 2µH to 500 µH. A comparison how the size of the inductor affects the return current and the output voltage in time is shown figure 4.5.

Since the Inductor would be fabricated via a large meander geometry, it's footprint is by far the largest of any involved elements. For the presented circuit with $L_1 = 100\mu H$, the footprint would be 148 x 148 μm^2, estimated via the meander geometry introduced in 4.1.

Performance of Circuit 1

The performance of the circuit for different inductor and resistor values is given in table 4.2. For the presented example of $L_1 = 100\mu H$, the peak voltage is $V_{out} = 145mV$ and the

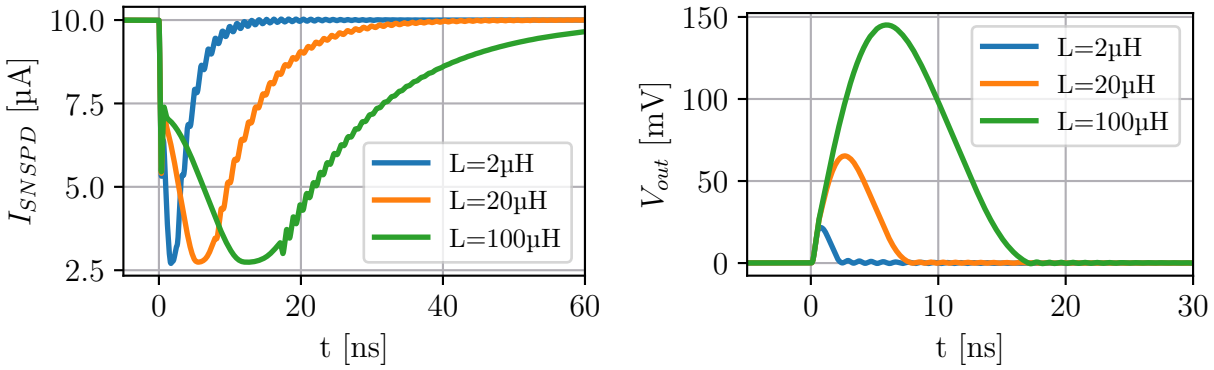

Figure 4.5: Effects of L_1 on Circuit 1

detection reset time is $\Delta t_{90} = 45$ns. The voltage is thus indeed two orders of magnitude larger than the voltage usually associated with SNSPD readout circuits. One reason for this increase is that there is no longer any connection to a 50 Ω line required. This isolation allows the circuit to build up much higher internal impedances and voltages.

For $L_1 = 500$µH the peak voltage would even reach $V_{out} = 322$ mV with a reset time of $\Delta t_{90} = 101$ns. However, this also requires a larger meander inductor. But in principle, at least via simulation, there does not seem to be a hard upper limit as to how far one could increase L_1 and thus also the output voltage.

We note that the possibility of SNSPDs gaining highly elevated resistances is widely known in the field, but for application at times directly dismissed as unrealistic and not reachable. To quote Berggren on this topic: "it is unlikely any signal present in a typical nanowire circuit would suffice to drive the system into this state" [57]. The reason presented is the presence of 50 Ohm transmission lines that for electrical readout are a necessary part of the circuit. However for optical readout, this restriction disappears, no 50 ohm line connects to the circuit anymore. With this limitation gone, the snspd can ideed be drivn even with passive circuits into much higher resistances and still reset afterwards.

The absence of the 50 Ohm connection might thus be one of the biggest benefits that optical readout provides. The isolation from any external low impedance opens up the possibility for circuit designs with much higher internal voltages, and new interaction strategies with the SNSPD.

LTspice simulation parameters for the nanowires

The properties of the NbN-Nanowires that I simulate across the three circuits are reported in table 4.3. This table contains also the properties for the following nanowires for circuit 2 and circuit 3, for compactness all listed together.

Table 4.2: Performance of Circuit 1 for different parameter pairs (L_1,R_1)

L_1	$R_{1,\max}$	V_{out}	Δt_{90}	Footprint
500 µH	15.8 kΩ	322 mV	101 ns	332x332 µm^2
100 µH	7.1 kΩ	145 mV	45 ns	148x148 µm^2
50 µH	5.0 kΩ	103 mV	32 ns	105x105 µm^2
20 µH	3.2 kΩ	65 mV	20 ns	66x66 µm^2
10 µH	2.2 kΩ	46 mV	15 ns	47x47 µm^2
5 µH	1.6 kΩ	33 mV	10 ns	33x33 µm^2
2 µH	1.0 kΩ	22 mV	7 ns	21x21 µm^2

Table 4.3: The parameters of all NbN-Nanowires in this chapter. Apart from the lengths (only reported for completeness) these are also the parameters given to LTspice.

	SNSPD (all circuits)	**Line** (Circuit 2)	**Line** (Circuit 3)	**Channel** (Circuit 3)
I_c	11 µA	62 µA	29 µA	120 µA
L_{kin}	300 nH	30 nH	50 nH	30 nH
w	100 nm	402 nm	204 nm	750 nm
l	60 µm	24 µm	20 µm	45 µm
$R_\square$	500 Ω/□			
T_c	10 K			

4.4 Circuit 2: Voltage amplification via cascading

In the second circuit, I introduce cascading to further increase the output voltage. The relation $V_{out} = Q/C$ suggest that the output voltage should increase to a first approximation linearly with the increase in available bias current.

The circuit is shown in figure 4.6, and the LTspice simulation is given in figure 4.7. I keep an inductor and a resistor as a sink path as as they turned out useful in the first circuit.

We chose an asymmetrical cascading design, where only one additional nanowire is put in parallel to the SNSPD, but which has a ca. 6x times larger critical current. As I model every SNSPD with a critical current of $I_c = 11\mu A$, the new parallel nanowire is chosen to have a critical current of $I_c^{(L)} = 62\mu A$. Via equation 2.7 We see that such a critical current is provided by a nanowire of width $w = 402$ nm. I call it from now on Line, since fabricating such a nanowire is simplest if it is just a straight line. There is also no other geometric requirement to this parallel nanowire, as it itself will not do any photo detection.

Each nanowire needs to be biased close to it's respective critical current. To split up the bias current, I put a resistor in series of each nanowire, setting the resistance ratio to 1:6. The overall source current is set to $I_0 = 70\mu A$. This way, the SNSPD is biased at $10\mu A$ (91%) and the Line is biased at $60\mu A$ (97%).

We choose such an asymmetric design because it might allow a more robust fabrication. One wide nanowire strip might be easier to fabricate than five or six thin ones which all have to turn out almost identical. This asymmetrical design does however introduce the need for the splitting resistors, it would thus be up to the actual fabrication to see which approach is better.

Detail on the Inductances

An detail of this cascading setup is that also the inductance of the Line has to be chosen relative to the inductance of the SNSPD, such that current is distributed evenly between them when the source current first starts flowing. I found that an inductance in the range $L_{Line} = 20 - 60$ nH work, and I chose here $30\mu H$. The inductance of the Line can be controlled in fabrication directly via it's length. In this case, the required inductance would result in a length of 24µm, also reported in table 4.3.

Performance of Circuit 2

The performance of circuit 2 for different circuit parameters is given in table 4.4. For $L_1 = 50\mu H$, the maximum output voltage is $V_{our} = 462$ mV with a reset time of $\Delta t_{90} =$ 88ns. The footprint of the inductor would be in this case 607x607 μm^2. The footprints for this cascaded circuit are considerably larger than for the first circuit, because here the meander inductor has to transport up to $70\mu A$ of current instead of only $10\mu A$.

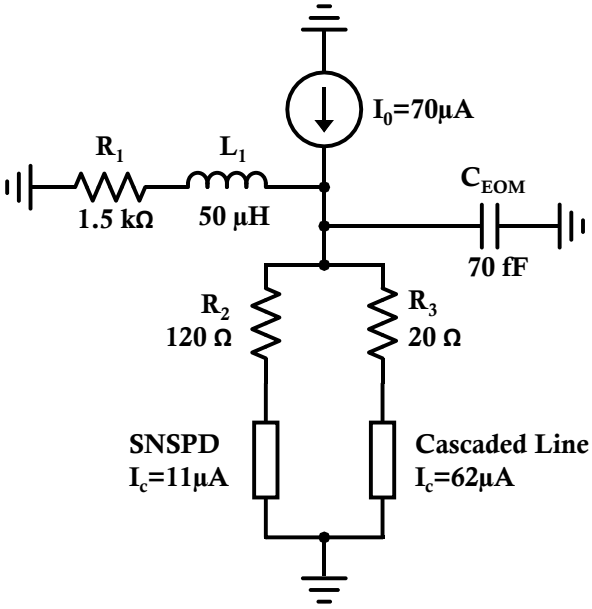

Figure 4.6: Circuit 2: SNSPD + Inductor + Cascading

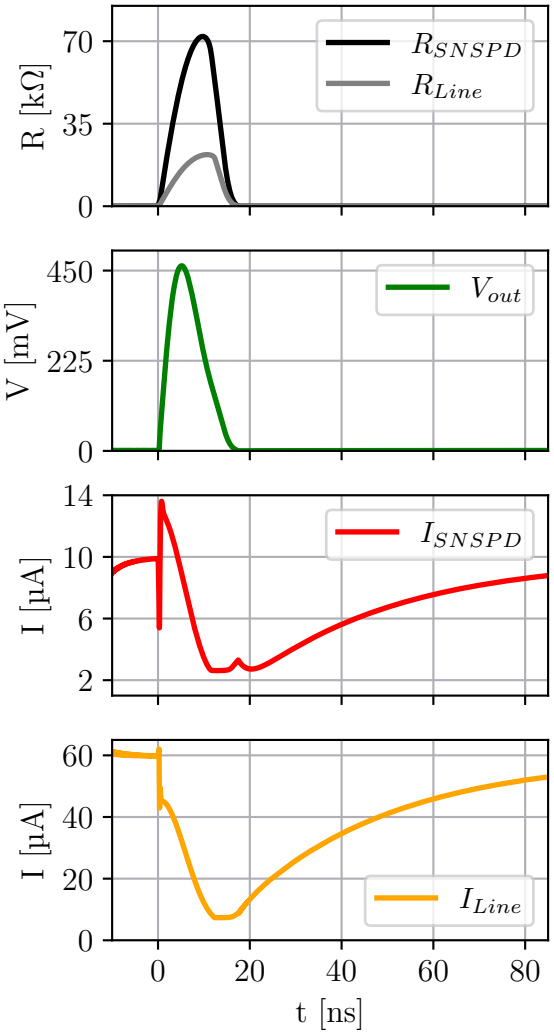

Figure 4.7: LTspice simulation of Circuit 2

Table 4.4: Performance of Circuit 2 for different parameter pairs (L_1,R_1)

L_1	$R_{1,\max}$	V_{out}	Δt_{90}	Footprint
50 µH	1.5 kΩ	462 mV	88 ns	607x607 µm^2
20 µH	0.9 kΩ	293 mV	58 ns	385x385 µm^2
10 µH	650 Ω	206 mV	41 ns	272x272 µm^2
5 µH	450 Ω	143 mV	30 ns	192x192 µm^2
2 µH	300 Ω	88 mV	19 ns	121x121 µm^2

4.5 Circuit 3: Voltage amplification via a thermal switch

In this third (and last) circuit, I investigated whether a thermal switch (as introduced in chapter 2) could be used to further increase the performance of an interfacing circuit. Such a switch would be electrically connected in the following way: The superconducting section would be connected in series with the sink path, i.e. with R_1 and L_1, while the heating element would be connected in series with the SNSPD and the Line. The complete circuit design is given in figure 4.8, and the predicted time evolution in figure 4.9.

The cascaded Line for this circuit is set to $I_c = 29\mu A$ and the source current to $I_0 = 38\mu A$. During iterative attempts at this circuit an additional resistor R_4 was required in parallel to the rest of the elements to provide an intermediate current sink to prevent latching. The values of L_1 and R_1 have also been refined through multiple attempts to their now shown values.

We will call the superconducting NbN-strip from now on "channel", and the resistive Ti-layer "heater". Shown in circuit schematic and inset in figure 4.8, I identify currents I_{ht} and I_{ch} in the circuit, which can then be mapped to be the currents inserted for thermal simulations.

For the design of the thermal switch, I chose the topheater design as presented in chapter 2 (with no cladding), and also chose the same dimensions as presented there[1], listed there in table 3.5. For the length of the NbN-strip, I choose 60 squares, such that when the channel is completely resistive it would have a resistance of 30kΩ.

The design of the circuit is motivated by the following idea: During steady state operation, the channel would be in a resistive state, due to continued heating by the heater. Right after the SNSPD clicks the channel would still be in a resistive state, providing a high resistance which helps in pushing charge into the EOM. However, since the current through SNSPD and Line is reduced after a photon absorption the heating current is reduced (observation in circuits 1 and 2 shows a reduction to half) and the heating power is quadratically reduced (joule heating scales with I^2R). This might allow the channel to cool enough to reach superconductivity. At that point it could then provide suddenly a very low-resistance sink for the current, allowing the SNSPD to reset. Finally, current returning into the SNSPD and Line would mean also again more heating, returning eventually into the steady state of a resistive channel.

One of the key question for simulation was, whether the channel would indeed return to superconductivity, and if the time scale would be fast enough before the SNSPD latches.

[1]The causation is of course the reverse one. After this particular heater design did show promising results in connection with this interfacing circuit simulations, I choose it also as the exemplary geometry for a general Topheater.

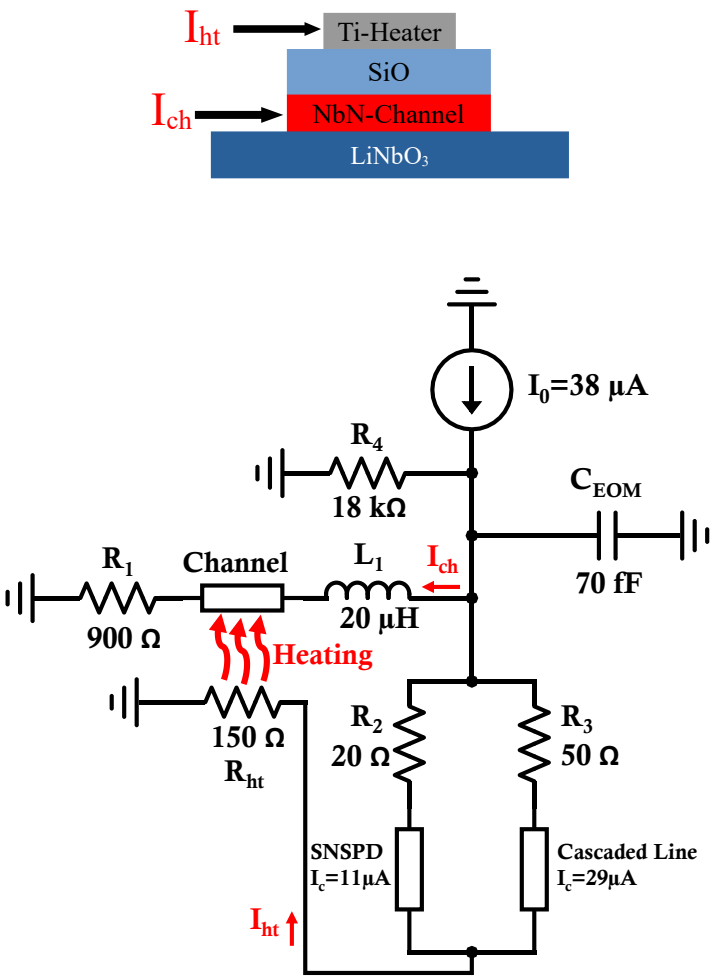

Figure 4.8: Circuit 3

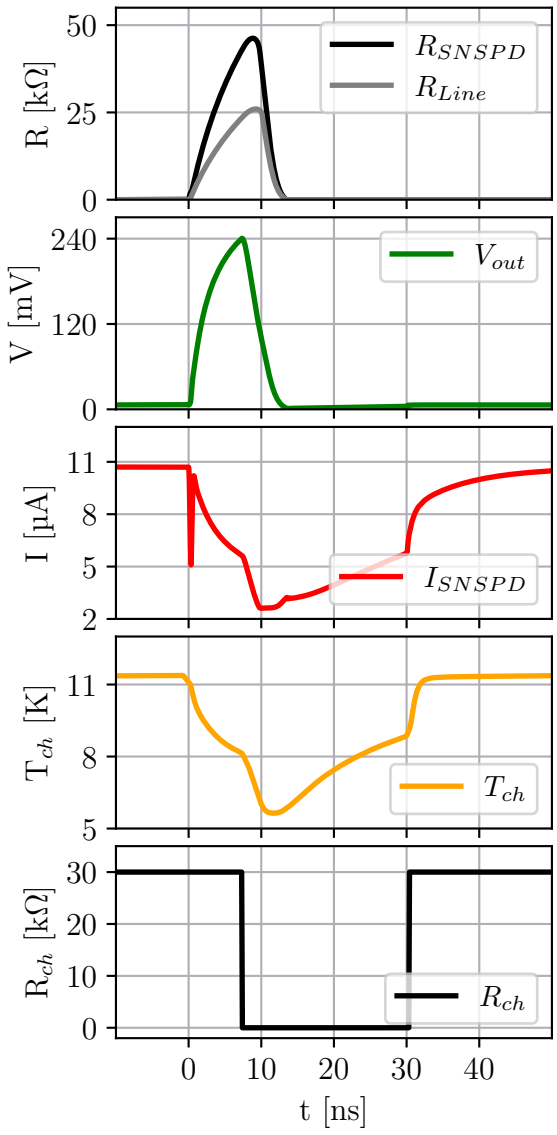

Figure 4.9: Predicted time evolution of Circuit 3

Strategy of predicting the time evolution

We use LTspice, Comsol, and the Ginzburg-Landau Equation $I_c(T)$ to progress forwards in time, stepwise per domain. I do simulation in one domain (Electrical, Thermal, or Theoretical) and then carry the result by hand (or by text file) into the next domain where they serve as the new input parameters.
One full prediction rotation visiting all three domains consists of:

1. Simulate the initial "cold" circuit in LTspice. Obtain some first time-dependent currents $I_{ht}(t)$ and $I_{ch}(t)$.

2. Simulate in Comsol the temperature evolution $T(t)$ of the channel, using $I_{ht}(t)$ and $I_{ch}(t)$ as the inputs for the heater and channel current.

3. See in a plotted graph whether $I_c(T(t))$ or $I_h(T(t))$ do at some point in time cross with $I_{ch}(t)$, using as inputs $T(t)$ and $I_{ch}(t)$. This checks whether the actual current in the channel reaches either the critical or the hysteresis current. If this is the case, read of the point in time where this crossover happens, i.e. where theory predicts a sudden change in the channels resistance. For the temperature-dependent hysteresis current I take the estimation $I_h(T) = 1/4 I_c(T)$, motivated by the ratio found in the previous LTspice simulations.

4. Insert in LTspice the newly found timestamp where the channel is predicted to change it's resistance. Do now a new simulation in LTspice, which now can electrically react to the change in time of the channels resistance.

The time evolution

It took 15 manual steps to solve the time evolution of circuit 3, at which point it returned to it's initial steady state. The steps are listed in compressed form chronologically in table 4.5, and will be now be commented each shortly.

- **Steps 1-5, Steady State:** The bias current Ib=38µA starts to flow. LTspice shows that the heater current is 31.8µA (the remaining 6.2µA flow initially through the still superconducting cold channel). Using this, Comsol shows that the channel heats up from 2K to 10K with 0.6ns. Add in LTspice that from t=0.6ns onwards the channel has resistance 30kΩ. LTspice now shows that the new steady state heater current is 37.4µA. With that, Comsol shows that after 100ns the channel has heated up to a plateau of 11.4K, with slow further heating. For much longer times it reaches temperatures up to 12.5K, but for our purpose I take 100ns as typical inter-photon arrival time and let a photon hit after 100ns of steady state heating.

- **Steps 6-9, Photon hits:** Simulate a photon hit in LTspice and define it as time t=0. Obtain Iht(t) (fig.4.10 left) and see that the heater current drops to about half the initial value immediately, and from there on keeps dropping further. Obtain also Ich(t), see that it slowly starts increasing. Insert both into Comsol, it shows that the channel temperature starts decreasing rapidly (fig 4.10 center). As the

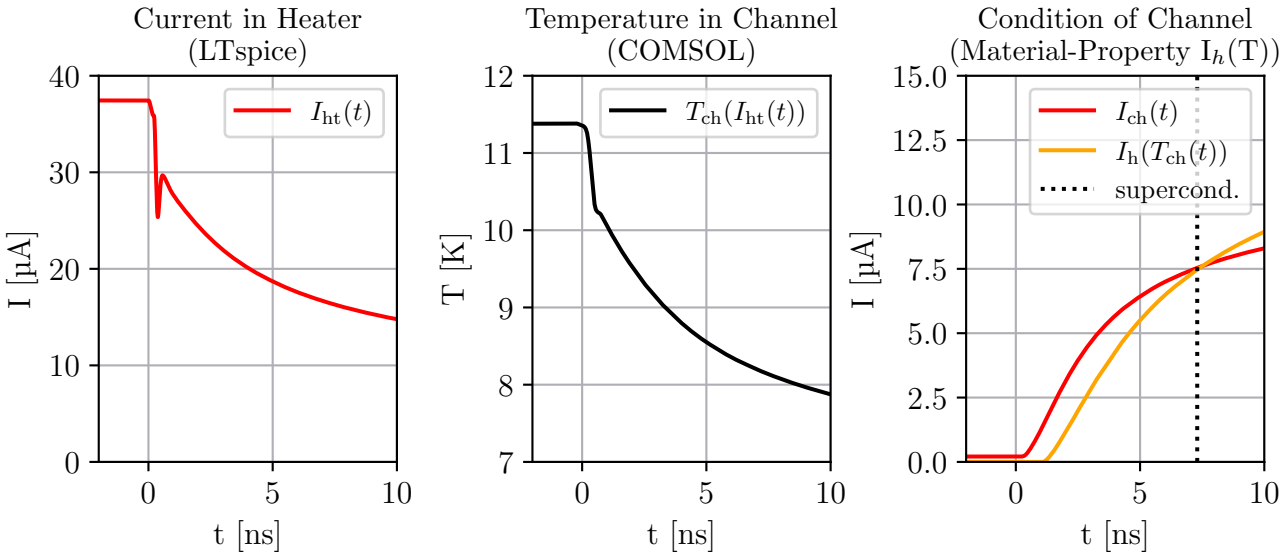

Figure 4.10: Steps 7-9 in determining the time evolution of Circuit 3.

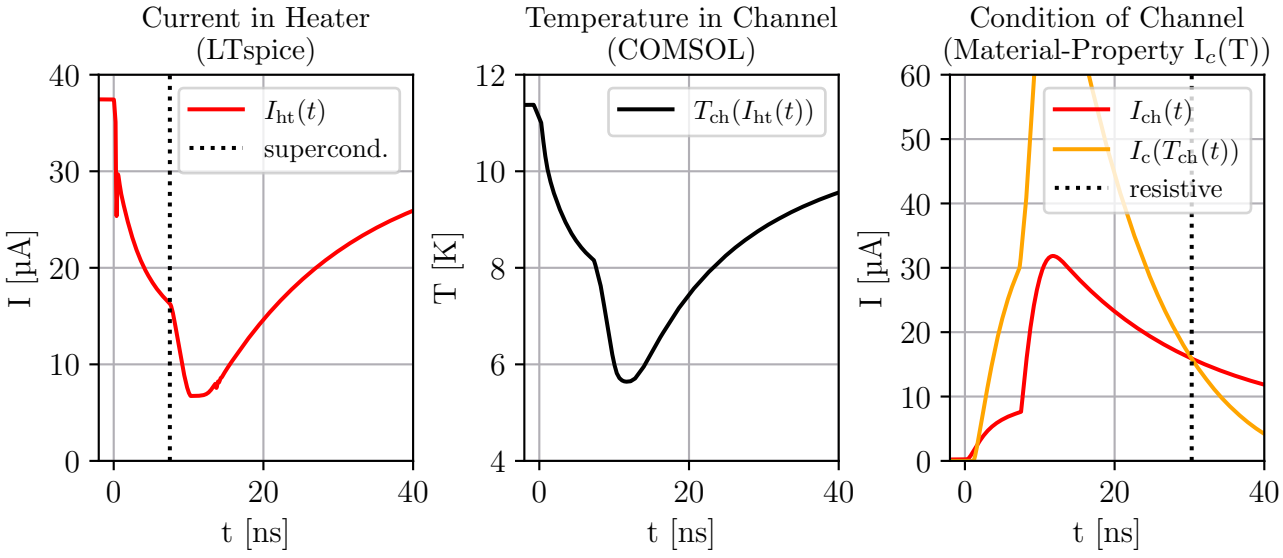

Figure 4.11: Steps 10-12 in determining time evolution of Circuit 3.

channel cools down, it can support more and more critical current. At t=7.3ns, the temperature-dependent hysteresis-current $I_h(T(t))$ rises above the channel current $I_{ch}(t)$ (fig. 4.10 right). Since the channel current is now lower than the hysteresis current, theory predicts that the nanowire becomes superconducting.

- **Steps 10-12, Circuit recovers:** Run LTspice again with the new information that at t=7.3ns the channel looses it's resistance. Shows that even more current flows through the sink path, and that the SNSPD is able to to reset into a superconducting state at around t=13ns (vanishing resistance at that timestamp in fig. **??**). Take the currents shown by LTspice (fig. 4.11 left) into Comsol, it shows that the channel heats up again (fig. 4.11 center). A warming channel can support less and less current, track $I_c(T(t))$ and see that it drops below $I_{ch}(t)$ at t=30.3ns: the channel becomes resistive again (fig. 4.11 right).

- **Steps 13-14, Return to Steady State:** Run LTspice with the new information that at t=30.3ns the channel has resistance 30kΩ again. Shows that at ca. t=45 ns the current in the SNSPD returnes to 90% of it's initial value. Taking the currents into Comsol, it shows that the channel returns to it's quasi-steady-state temperature of around 11.4K even quicker, at around t=34ns. Since the biasing of the SNSPD is the relevant factor for photon sensitivity, I conclude that from ca. t=45 ns onwards the circuit is ready for the next photon detection. Show the now fully known time evolution from all domains combined (figure 4.9).

Performance of Circuit 3

Circuit 3 has a peak voltage output of $V_{out} = 240$ mV and a reset time of $\Delta t_{90} = 45$ ns, as shown in the time-evolution in figure 4.9.

Compared to the other two circuits, however, there is no clear way how to scale this performance into a higher value (i.e. by just increasing the inductor value). Changing any one element or parameter in circuit 3 in almost all cases destroys the reset dynamics and leads to latching, due to the high degree of self-feedback and so many moving parts.

Table 4.5: Manual determination of the time evolution of Circuit 3

Step	**Time**	**Using**	**New Result**	**Figure**
1	Initialize	-	$I_0 = 38$ µA	-
2		LTspice	$I_{ht} = 31.9$ µA	-
3		COMSOL	Channel becomes resistive $T_{ch} = 10\text{K} \Rightarrow R_{ch} = 30$ kΩ	-
4	Steady State	LTspice	$I_{ht,steady} = 37.4$ µA	-
5		COMSOL	$T_{ch,steady} = 11.4$ K (timescale $\sim$ 100ns)	-
6	0 ns	LTspice	Photon hit at $t = 0$	-
7		LTspice	Cascading $I_{ht}(t)$, $I_{ch}(t)$	Fig. 4.10
8		COMSOL	Cooldown $T_{ch}(t)$	Fig. 4.10
9		$I_{re}(T)$	Channel becomes superconducting $I_{ch} \leq I_{re}$ @ 7.5 ns	Fig. 4.10
10	7.5 ns	LTspice	Returning $I_{ht}(t)$, $I_{ch}(t)$	Fig. 4.11
11		COMSOL	Heating $T_{ch}(t)$	Fig. 4.11
12		$I_c(T)$	Channel becomes resistive again $I_{ch} \geq I_c$ @ 30.3 ns	Fig. 4.11
13	30.3 ns	LTspice	Full $I_{ht}(t)$, $I_{ch}(t)$	Fig. **??**
14		COMSOL	Full $T_{ch}(t)$	Fig. **??**
15	$\sim$45 ns	-	ready for next photon to hit	-

4.6 Conclusion of Chapter 4

We presented three new circuits which could be used for interfacing an IR-sensitive SNSPD with a LiNbO3-Racetrack-Resonator for use of optical readout.

Circuit 1 consisted of one added inductor, following intuitions about the behaviour of the individual circuit components. It had a peak output voltage of 145mV with a reset time of 45ns, with possibilities of further voltage scaling to 322mV and beyond if the reset duration is allowed to be longer.

It was surprisingly effective, given that the change to the circuit was relatively minor. Also, the the reset requirements were robust against changes of any single element parameters, making it a promising candidate for fabrication.

The isolation from any 50 Ohm line was seen as one of the main reasons this circuit could create such high voltages, two orders of magnitude higher than in 50-ohm-connected circuits. The current could be pushed for a much longer duration into the SNSPD, growing it's resistance up to 33kΩ, which resulted the large charge accumulation at the EOM, providing the high output voltage.

Circuit 2 consisted of an additional cascading scheme, which had been adapted from similar demonstrations in literature. It had a peak output voltage of 462mV with a reset time of 88ns, also with possibilities of further voltage scaling. To achieve the cascading, multiple devices had to be within specific parameter ranges, making fabrication still a

possibility, but now with the requirement of good previous characterisation. The footprint required is considerably larger than for circuit 1 due to the larger meander inductor. Overall, not many new insights compared to circuit 1, but it showed that the techniques used in circuit 1 still work also under cascading.

Circuit 3 consisted of an additional thermal switch which interacted with the circuit in a highly self-coupled manner, which to my knowledge as not been reported in literature before. The closest match might be [79], but there without self-feedback. It had a peak output voltage of 240mV with a reset time of 45ns, only being comparable to the performances of the other circuits, but not better. It was much more difficult to simulate than the previous circuits. LTspice, Comsol and theoretical models had to be combined in a 15-step manual process to reconstruct the time evolution. The circuit was also extremely fragile, as any one parameter change generally destroyed the reset property and led to latching. It took time to find this one parameter set where the reset did work, showing also no clear pathway of scaling for a particular figure of merit.

Out of all the circuits, Circuit 1 was overall the biggest surprise. With only a minor change to a known default circuit it allowed to increase the output voltage by two orders of magnitude, while only needing one large meander as a new relevant geometry for fabrication. With an output voltage of up to 322 mV with large inductors, it reached the regime of 460 mV which I estimated for successful optical readout. The employed SNSPD was of the typical IR-sensitive regime, and the reset time of 45ns could translate into a count rate of up to 20 MHz. The most direct available comparison in literature is the work by de Cea [22], where the detection is limited to UV-photons and the reset time is on the order of 1µs, giving rise to maximum count rates of only 1 MHz.

We end with an observations already presented for circuit 1: The absence of the 50 Ohm connection might be one of the biggest benefits that optical readout provides. The isolation from any external low impedance opens up many new possibilities or circuit design, where much higher higher internal voltages are possible, as well as new interactions between circuit and SNSPD.

Chapter 5

Experiments

In this final chapter, I report on the fabricated and measured chips during this thesis. They were designed to test experimentally some of the structures I took for granted during theoretical modeling.

Three chips that I fabricated and measured. Two in regards of thin film resistors, and one in regards of NbN critical currents. I first introduce the experimental methods and then present the result and discuss them.

5.1 Experimental Methods

The experimental methods contain three consecutive stages: Chip-Design, Fabrication and Characterisation.

A chip needs to be first designed and a final design file generated. Then, multiple fabrication processes are employed to pattern the designed geometries physically on the chip. Eventually, the chip can be characterized by imaging techniques for geometric parameters, and via electronic measurements to extract material and device parameters.

Chip-Design via *gdshelpers*

Chip-Design is initiated at the computer, within our group most often in python with the help of the library *gdshelpers*. It allows to make use the flexibility of python in defining and constructing all the desired shapes.

Often semi-automated shape generation is employed for parameter sweeps. One template design is created and then copied to fill a whole row or an array of similar devices, all identical up to some with some specific parameter that is swept. This technique is a robust way to find optimal design values when done iteratively with measurements.

The library allows to eventually export the design automatically in the GDSII format, a standard format for lithographic machines. For multi-step processes, local markers and region have to be defined near to each structure, such that the litographic machine can align itself each step to the previous structures.

The particular design is also heavily influenced by the physical processes that are employed in fabrication. If for example some process is known to create systematically

smaller nanowire widths than nominally given by the design, such systematic offsets can be compensated by already in design by adding the respective known offset to the designed shapes as well, such that the resulting chip will then have the actually desired physical dimensions.

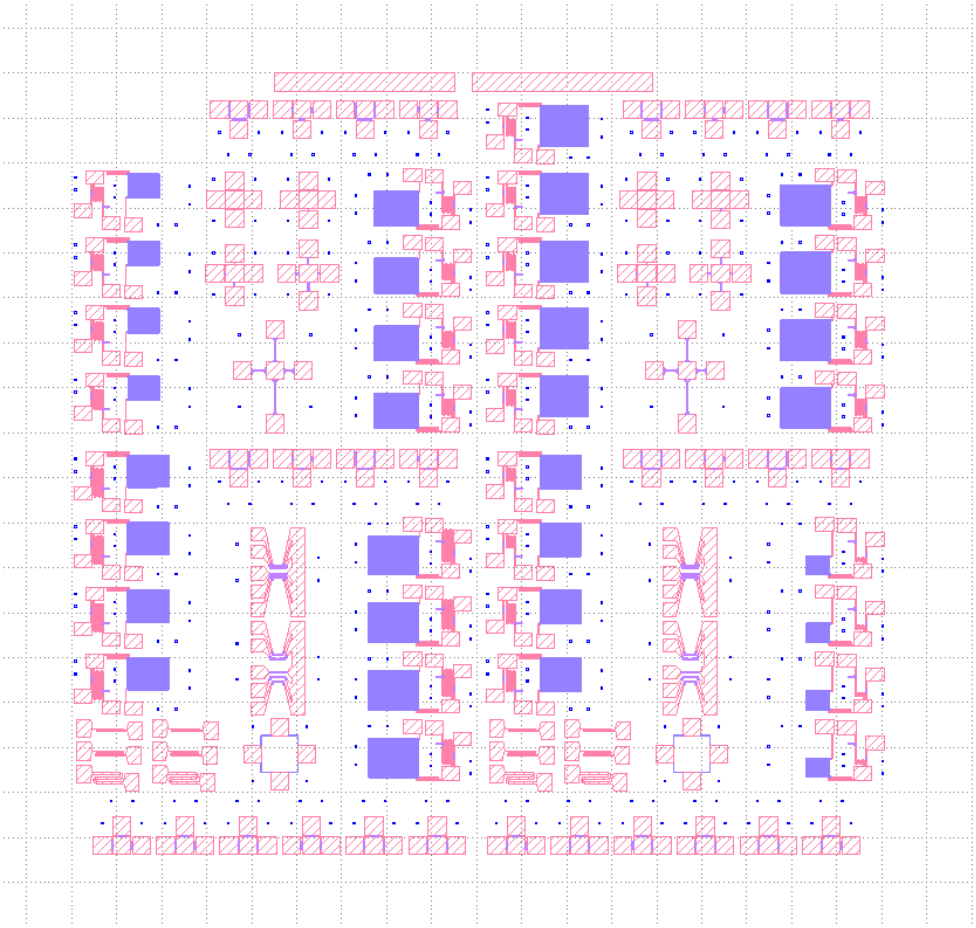

Figure 5.1: A view of a typical chip-design. Here for the fabricated NbN-chip. Red correspond to where Gold will be deposited, and violet to where NbN-nanowires will be etched.

Fabrication steps

Fabrication begins with the choice of a chip with a specific desired material stack. As shown in the introduction 2.2, a chip with all proposed structures for my purpose would need to consist of a stack of Si, SiO, LiNbO3 and NbN. However, for preliminary characterisation fabrication, one can resolve to reduced material stacks. A common chip stack consists of Si, SiO, SiN, because SiN is a popular waveguide material.

To add structures to the (initially blank) chip, a fabrication process of several physical steps is required. Most of these steps are for a large part almost the same every fab-

rication process, while the there is one exception towards the end: the choice between either an additive step (Deposition) or a subtractive step (Etching). The steps including deposition are shown in figure 5.2, while the steps including etching are shown in figure 5.3.

A fabrication process starts with the blank chip, which is first cleaned via Acetone and then heat-treated at ca. 100°C for some minutes, to remove any dirt or impurities. Then, a layer of resist is spincoated on top of the chip. A resist is a viscose fluid that is reacts chemically to the bombardment of electrons, which during patterning allow to change the chemical properties of the resist only at precisely defined locations. Spincoating is a process where the chip is put on a fast rotating stage (on the order of 2000 rpm), on which then the resist is dropped. The fast rotation spreads the resist evenly over the whole chip area, and reduces it's thickness to around 100-800 nm. Once the chip is spincoated, it can be loaded into the electron beam.

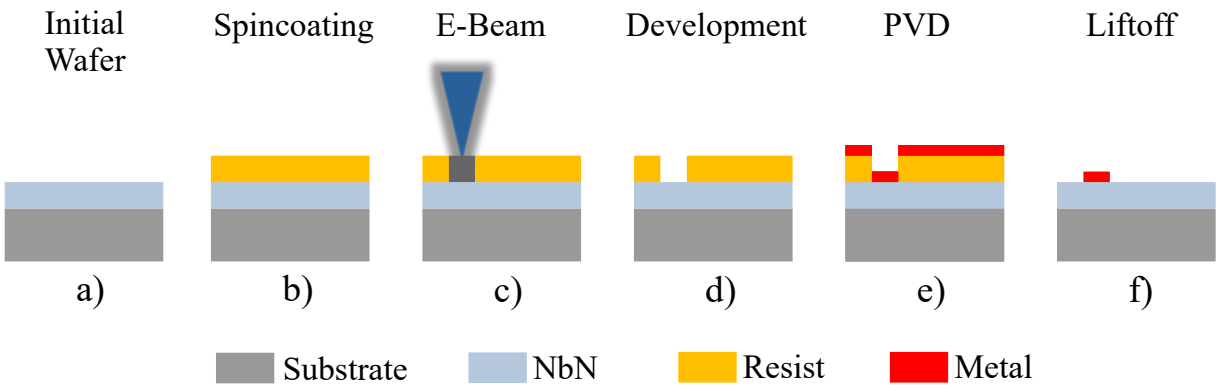

Figure 5.2: Fabrication-process with Physical-Vapor-Deposition

The electron beam (E-Beam) is a machine that can accelerate electrons up to the energy of 100kV, collimate them into a sharp beam, and then deflect the beam over the chip to any desired location. Due to the precise guiding and the small beam width of the electron beam, this allows a spatial control over the beams position down to the order of 10nm. The desired chip design can then be loaded into the E-Beam, where it then reads then the coordinates of the areas to irradiate. When at these selected positions the high energy electrons hit the resist, they locally change it's chemical makeup. This way, the information of the design is imprinted via the E-Beam into the resist on top of the chip. Depending on the resist this can decrease the available resolution, as the chemical change within the resist might not be exactly limited to the spot the electrons hit.

The next step is chemical development. The chip (with the patterned resist on top) is put into a developing bath. During this developing, those areas where the resist had been impacted by electrons are washed away, while the non-impacted areas of the resist remain intact. This is the case for a positive resist. There do also exists negative resists, which behave the opposite way, where only the impacted areas remain intact. The information

of the design is now encoded on whether resist exists or does not exist for each location on the chip.

An actual change to the chip itself happens in the now following step, where a choice between an additive process (deposition) or a subtractive process (etching) is available. Deposition allows to add a new material on top of the chip, while etching allows to strucure an already existing layer.

In my case, deposition is achieved via Physical-Vapor-Deposition (PVD), where a material is heated strongly enough that it's atoms are vaporized and settle as a thin film on top of a new surface. This can be used to deposit materials on top of the chip with nm-precision in height. Examples for typically deposited materials are Gold and Chrom, which are used to form electrical circuits on chips.

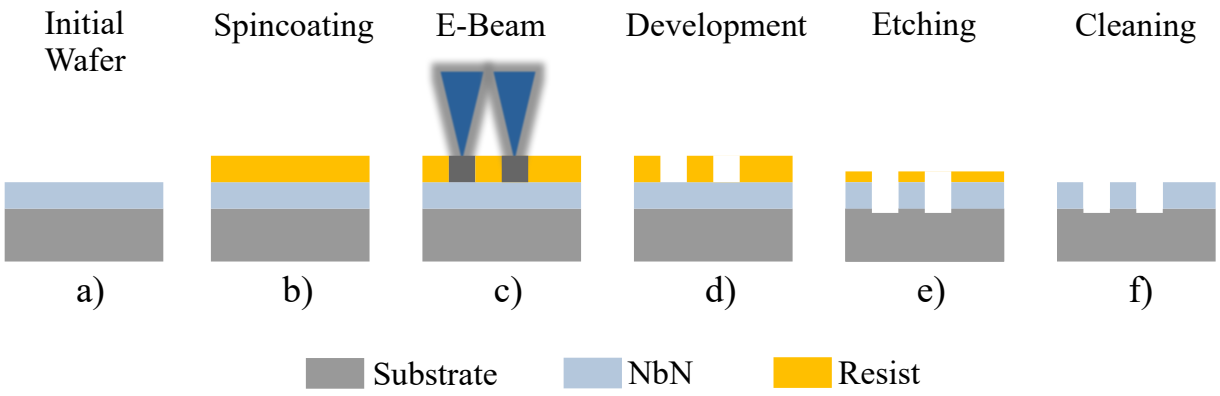

Figure 5.3: Fabrication-process with Etching

Etching is achieved via e.g. Plasma-Etching. The chip is put in a chamber with a plasma, where the kinetic energy of the atoms in the plasma hit on the the exposed areas of the chip and carve trenches into it. This allows to pattern a new structures into a material that already exists on the film, up to etching e trench completely through this material.

After either Deposition or Etching, a last chemical step is performed, called Liftoff. The chip is put into a chemical bath that washes away any remaining resist. In the case of Deposition, this also washes away any deposited material that was not in direct contact with the chip, i.e. those areas where the E-Beam did not hit the resists. After liftoff, one fabrication process is complete.

Depending on the desired structures on the chip, the fabrication process can now be repeated multiple times, for example by deposition a second material at different locations. The more fabrication iterations are done, the more complex the chip can be, but also the higher the risk that at any point an error occurs and the fabrication has to be started new

from the beginning.

Imaging techniques

During fabrication or after fabrication it is often helpful to image the resulting structures. This can be used to confirm that the fabrication proceeded as expected, or to detect unexpected changes on the chip.

Here, I list some of the most often employed imaging techniques and their respective typical use.

Optical Microscope

The optical microscope allows for a quick inspection of larger structures on a chip. It this can be done in a few minutes and can be done between almost any step during the fabrication. The resolution up to some µm. This is especially useful for the deposition step of larger structures like gold-pads or gold-wires. Before fabrication, one can also check for dirt or large impurities, which would indicate that more cleaning is needed.

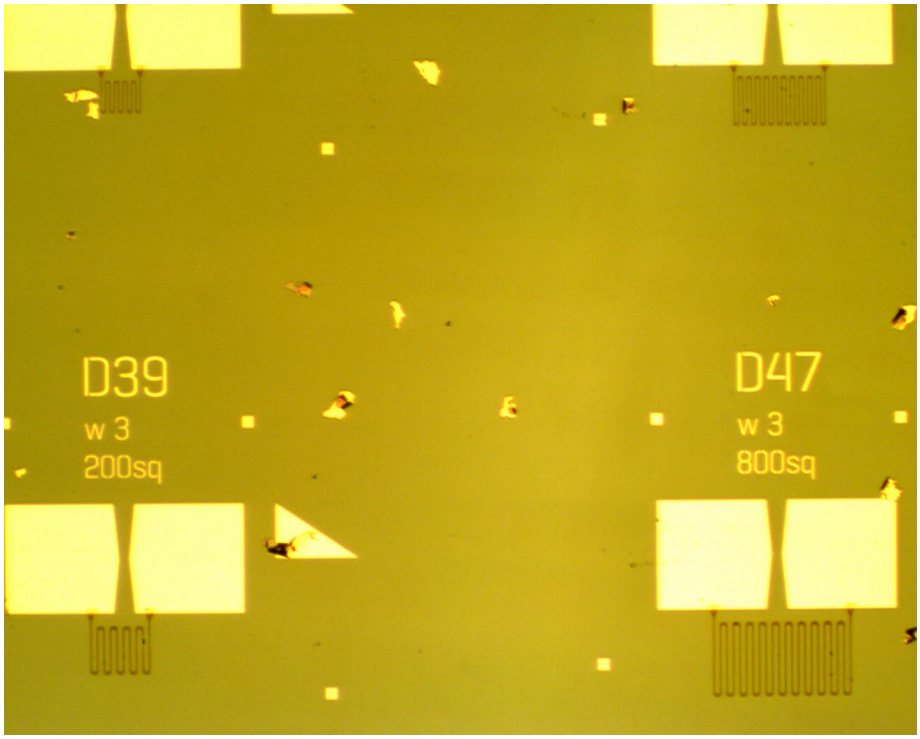

Figure 5.4: Optical Microscope Image of some of the fabricated resistors

Scanning Electron Microscope

The Scanning Electron Microscope (SEM) allows a much more advanced imaging method. The Chip is put into vacuum, and highly accelerated electrons are shot at it, probing it's local geometry. Using an SEM takes roughly 1-2 hours, including loading and calibration. An example SEM-Picture is shown in figure 5.5. It can resolve features down to ca. 10nm if

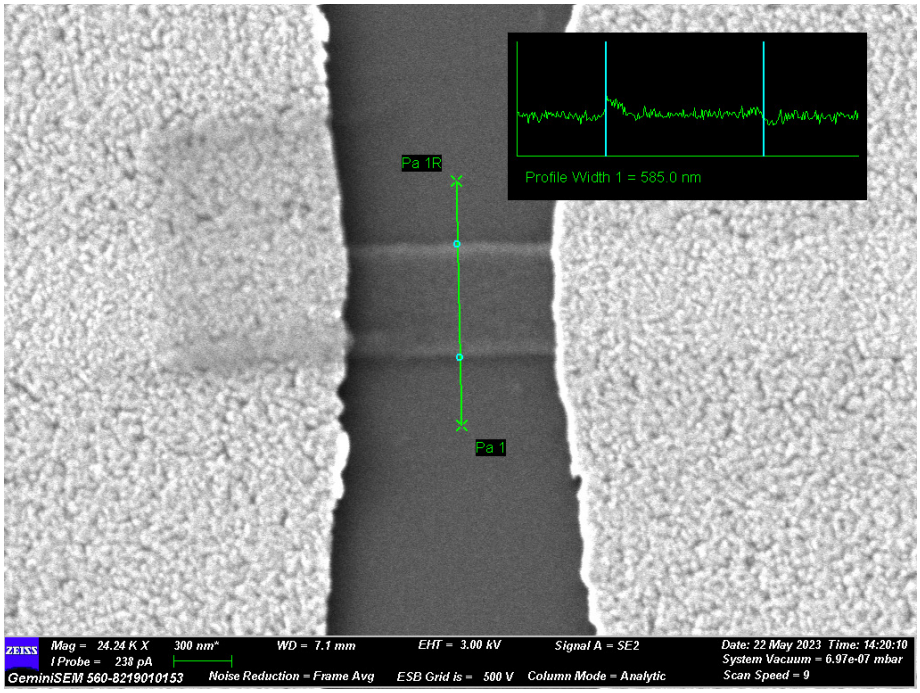

Figure 5.5: SEM-Image of a NbN strip

calibrated well. The smallest features on a typical photonic chip are usually the nanowires such as SNSPDs, with widths down to about 100nm, which thus can be imaged via an SEM. The SEM also usefull to check fabricated widths and lengths, and to compare them with the designed values. This can reveal systematic errors or shifts, that could then be compensated in a new design. A note: The Electrons that are used for imaging can still damage the chip, as they arrive with a high kinetic energy. It can happen that one is both imaging and damaging a chip in the SEM at the same time.

Profilometer

A profilometer is a device that has a very thin needle (tip radius on the order of ca. 1µm) that is scanned in a line over the chip. The tip is in physical contact with the surface of the chip and traces it's surface height. Resolution is possible down to 1 nm in height and 4 µm in lateral dimensions, making it especially useful for height measurements. A typical profilometer measurement is given in figure 5.6. It is operated at room atmosphere and a measurement of multiple lines over a chip can be done in ca. 10-30 minutes.

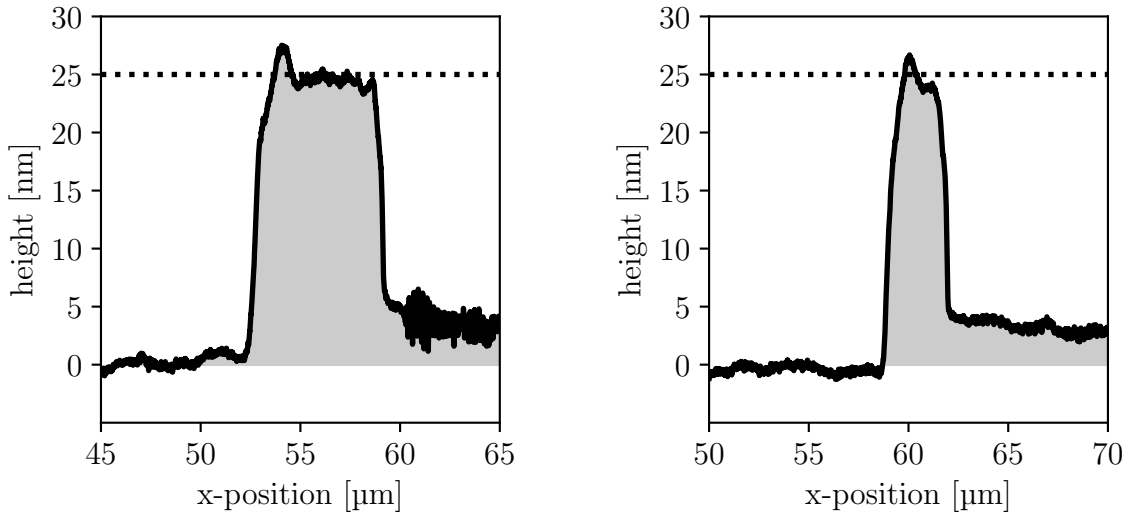

Figure 5.6: Profilometer measurements of two resistors on the Gold-Chip. The ca. 5nm offset to the right of each structure was determined to be most probably a hysteresis effect of the scanning tip.

Cryogenic Apparatus

The cryostat in which the measurements of this were conducted was a closed-cycle helium-cooled cryostat from Scontel (Model RDK-101DL). An initial rough vacuum is created via a scroll pump, reaching ca. 10^{-2}mbar, from there on a finer vacuum is created via a turbo-pump, reaching ca. 10^{-4}mbar. A closed-cycle helium compressor unit (CNA-11 from Sumitomo) is then employed for the cooldown, reaching a base temperature of 4 ± 0.1K after ca. 12 hours. Warmup of the cryostat takes around 36 hours, as it is done while still maintaining the vacuum. This reduces the potential danger of contamination, as already e.g. condensating water from the air can significantly degrade the performance of a cryostat. The cryostat offers access to the cryogenic chip via 16 coaxial and 26 DC connections. Since most chips have much more devices that coaxial lines are available, multiple cooldowns can be necessary to characterize on chip.

Printed Circuit Board

A printed circuit board (PCB) is often employed to interface between the cryogenic chip and the cryostat. The board is mounted on a cryogenic stage inside the cryostat, and the chip is then mounted on the board. For better thermal contact the chip can also be glued directly onto a metal holder, if a corresponding hole is designed inside the PCB. A photograph of a PCB with a wirebonded chip is given in figure 5.7.

The connection between chip and PCB is achieved via wirebonds, thin metallic wires that are pressed on both the chip and the PCB, providing enough adhesion and an electrical connection. On the chip, on needs to design dedicated bondpads of dimensions ca. 200 x 200 µm^2 to allow for easy access for the wirebonds. In figure 5.9 four of such bondpads

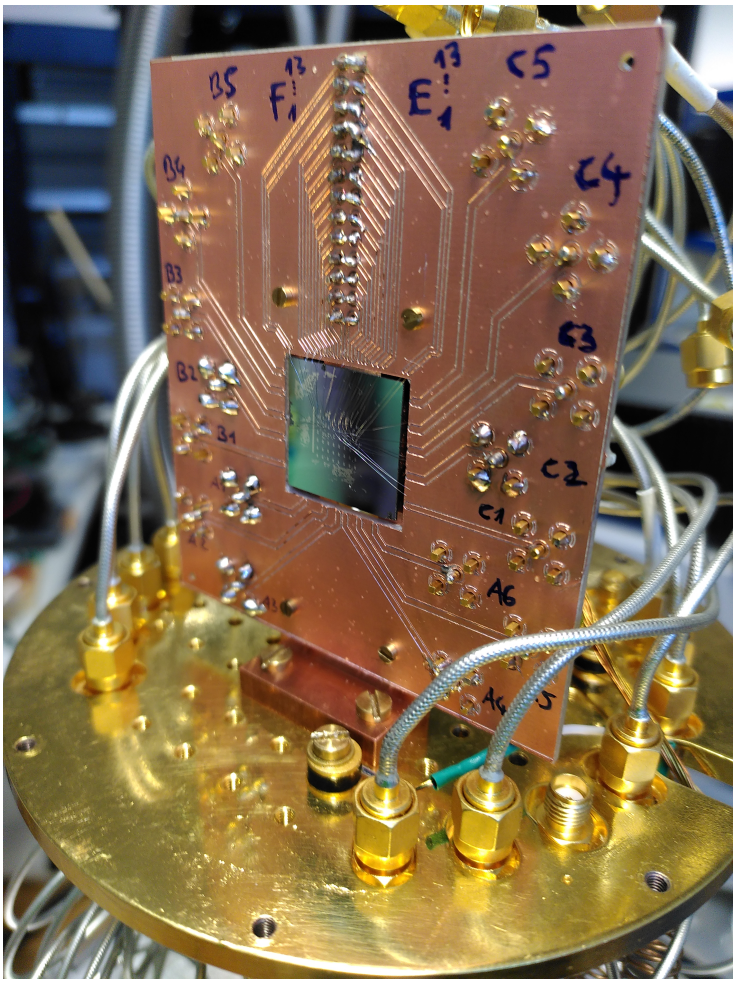

Figure 5.7: Photograph of a PCB mounted on a cryogenic stage and connected via SMA cables, with a chip connecting to the PCB via wirebonds

can be seen, which form the endpoints of the electrical circuit on-chip. On the PCB the signals from the wirebonds are routed via traces to the outer region of the PCB, where SMA-Connectors allow to attach a coaxial cable, which can then be used to route the signal through the electrical ports of the cryostat to the outside.

When designing a PCB for use for high frequencies (from ca. 100MHz and beyond), it is necessary to choose the widths and clearances of the traces such that they have a 50 Ω impedance. Otherwise, high reflection losses would appear between the PCB and any coaxial cable. Additionally, also bends and sharp corners should be avoided when designing RF traces. For DC traces, this is not an issue, they can be designed for any geometry.

The PCB shown in figure 5.7 was designed for this thesis and fabricated by the electrical workshop in the KIP. It used a standard single copper layer. When high quality transmission lines for RF signals in the GHz-regime are required, a multilayer PCB is preferred, where intermediate ground planes help keeping the dimensions small for a 50 Ω matching.

Standard electronic readout setup

To measure resistances of chips, the signal lines coming out of the cryostat were directly connected with an Agilent 34401A Digital Multimeter, with no further components in between.

To measure critical currents of NbN, a Keithley 2450 source-meter was employed. The complete setup is given in figure. The source voltage of the Keithley was routed through a 4 MHz lowpass filter, then through either a 1 MΩ or 150kΩ resistor, and then through a Bias-Tee to the feed through connectors of the cryostat. A sketch of the setup is given in figure 5.8.

To measure IV-Curves, the Keithley was set to voltage source mode. Together with the high resistors in series, this resulted in controlling the current reaching the devices on the chip, which provided a more stable current-source than directly sourcing current via the Keithley. The voltage was ramped up and down again in the range 0-30V, which for the 1MΩ resistor resulted in a scanned bias current of 0-30 uA.

By substracting the (precisely measured) resistance R_s of the 1MΩ resistors from the measured resistances R_{meas}, the resistance R_{dev} of the device under test could be calculated:

$$R_{dev} = R_{meas} - R_s \tag{5.1}$$

If larger bias currents than 30uA were required, the resistor in series was swapped for a smaller 150kΩ value. This allowed scanning bias currents up to 200µA, which was then sufficient for even the widest structures measured in this thesis.

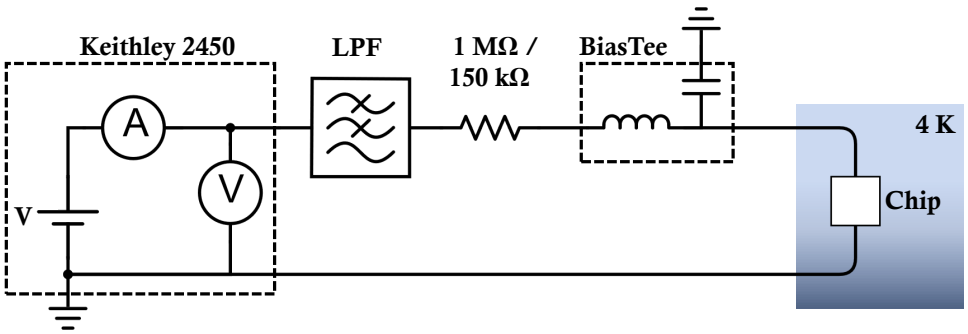

Figure 5.8: Electronic readout setup for measuring IV-Curves

5.2 Fabricated Chips

Three chips were designed and fabricated, two for the use as resistor measurements, on for the use of NbN critical current measurements.

Chips for resistance measurements

Two chips were designed for thin film resistance measurements. To this end, strips of widths between 1-4 µm and lengths between 1-800 sq were designed, with bondpads at

each end of a strip. For long strips, a meander geometry was employed to keep the two bondpads of the strip close together. A microscope image of four such resistors can be seen in figure 5.4.

The two chips designed for thin-film measurements were fabricated solely via deposition methods. As a wafer material, a base stackup of Si/SiO/SiN was used. Due to the respective deposited metals, I will refer to these two chips as Gold-Chip and Pd-Chip. Their fabrication process was:

- **Gold-Chip:**
  1.: Cr+Gold (10nm+10nm)
- **Pd-Chip**:
  1.: Cr+Gold (10nm+80nm)
  2.: Ti+Pd (4nm+5nm)

where for the Gold-Chip the deposition was 10nm Gold (with a adhesion layer of Chrom below). This was the only deposited layer, all structure on this chip was due to this deposited material. For the Pd-Chip instead, two depositions where done. First, 80nm Gold (with a adhesion layer of Chrome), and then in a second fabrication iteration 5nm Palladium (with an adhesion layer of Ti). The Gold layer was used to form bond-pads and electrical connections, while the Pd-layer was used to form the resistors.

Chip for critical current measurements

A third chip was designed for critical current measurements of NbN. To this end, three different main geometries were of interest: SNSPDs, Lines, and Meanders. The SNSPDs were fabricated with widths of 100nm and lengths of 40µm, 70µm and 140µm, to measure whether they were similar in properties to typical ones reported in literature. The Lines were chosen in widths from 100nm to 3µm to see whether their critical current would linearly increase with the width. The meanders were added to see whether such large structures could be fabricated without any degrading imperfections.

An impression of the complete NbN-chip design can be seen in figure 5.1, while a microscope image of a section of the fabricated chip is presented in figure 5.9, with annotations for each of the distinct structures.

The fabrication of the NbN-chip started with a waferstack of Si/SiO/SiN/NbN. A wafer was chosen that had a 5nm thin NbN-film already deposited on top. The fabrication process from there on was:

- **NbN-Chip**:
  1. Cr+Gold (10nm+80nm)
  2. NbN (40ns) Etching

The etching was sufficient to completely etch through the NbN-layer, while still keeping the Gold-Layer intact for the electrical wiring.

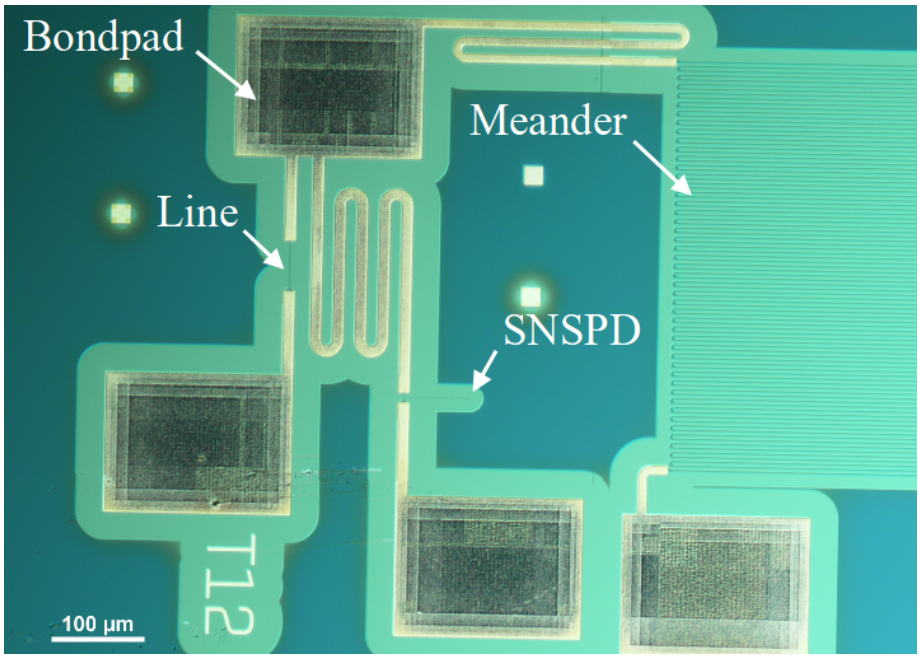

Figure 5.9: Microscope Image of part of the NbN chip

5.3 Results

We report now the resistance measurements for Gold and Palladium, and the critical current measurements for NbN.

Resistances of Gold

The Gold-chip was fabricated to be nominally 20nm height. Profilometer measurements however gave for multiple parts across the chip a total height of 25nm. Two representateive height profiles are given in figure 5.6. The measurements were done scanning from low to high x-position.

At the falling right edge of the structure, it can be observed that the height profile does not return to the initial height but to a ca. 5nm elevated level. When turning the scan direction around, the same 5nm offset in the measurement appeared, but now at the other physical side of the strip. I thus attribute the falling edge offset to a hysteresis effect of the profilometer, and take the rising edge height of 25nm as the actual height of the chips. Gold-depositions are often done in batches of multiple chips, as was also this chip. The 10nm Chrom adhesion layer is deposited first, for all chip together, and then varying thicknesses of gold are added for each individual chip.

We assume that the most likely difference accounting between planned and actual height is due to a slightly too long deposition of Gold, of 15nm instead of nominal 10nm, on top of a standardized and most likely correct 10nm Chrom layer.

The measured gold resistances, standardized per square, are reported in figure 5.10. At cryogenic temperatures of 4 K, I find $R_{Au} = 4.3 \pm 0.2\ \Omega/\text{sq}$, while at room-temperature for the same devices I get a higher resistance of $R_{Au} = 6.2 \pm 0.2\ \Omega/\text{sq}$. Normalizing by

the height of $h = 15$nm, the resistivities $\rho = R_{sq} \cdot h$ result in:

$$\rho_{Au}(4K) = 64\ \Omega\,\text{nm}$$
$$\rho_{Au}(300K) = 93\ \Omega\,\text{nm}$$

The literature values I found for gold on the other hand, for the cryogenic case, where around $\rho_{Au,Lit}(2K) = 10\ \Omega\,\text{nm}$ (see parameter collection 3.2.4). My resistances are a factor 6 larger.

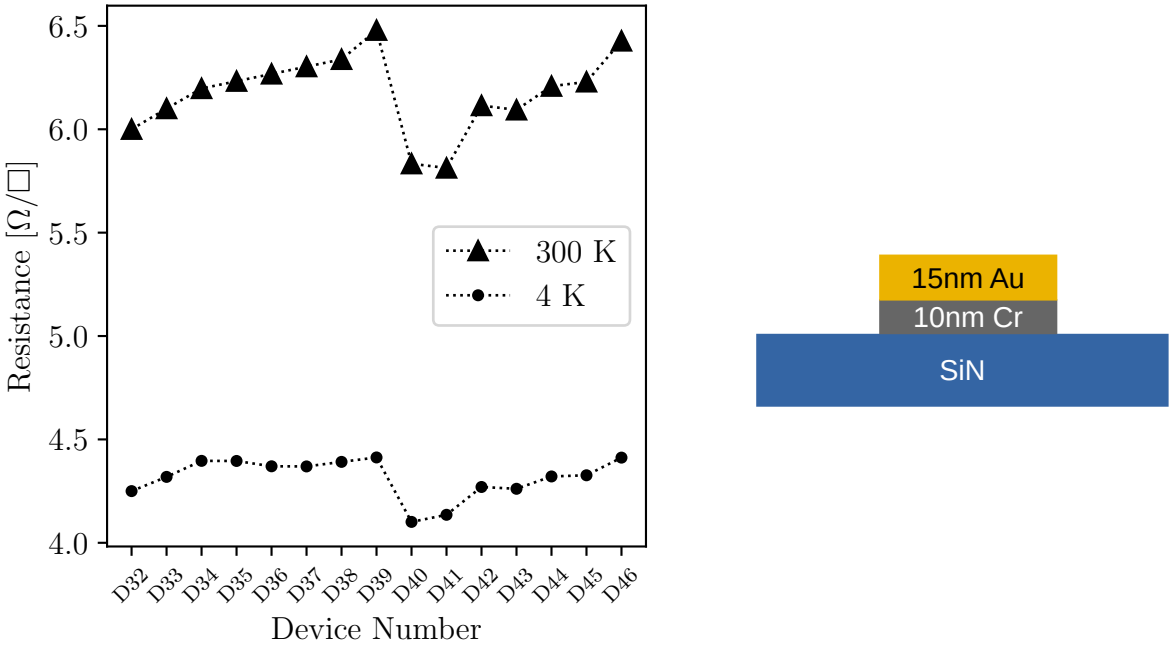

Figure 5.10: Gold Resistance for shown Stackup

Resistance of Palladium

The measured resistances at 4K of palladium are given in figure 5.11. The plot shows that most data points lie close together in range, with some distinc outliers.

Closer inspection revealed that the high-resistance datapoints stemmed from resistors with only 1-5 squares length, which completely distored their measurement, as already half a bondpad can add half a square of resistance. It was thus an error in design to fabricate the lengths down to 1sq. Additionally, also resistors below 1µm width varied more strongly in their resistance value.

When I retain only resistors with lengths of at least 10 squares and widths of at least 1µm in the data set, the remaining points show a much more homogeneous distribution, given in figure 5.12, varying now from 65 Ω/sq to 85 Ω/sq.

Within this set, I can do a last selection of again the most robust data points, those of lengths at least 50sq and widths of at least 2µm. This last filtering results in a final square resistance of Palladium of $R_{Pd}(4K) = 78 \pm 2\Omega$/sq. The Palladium deposition had been

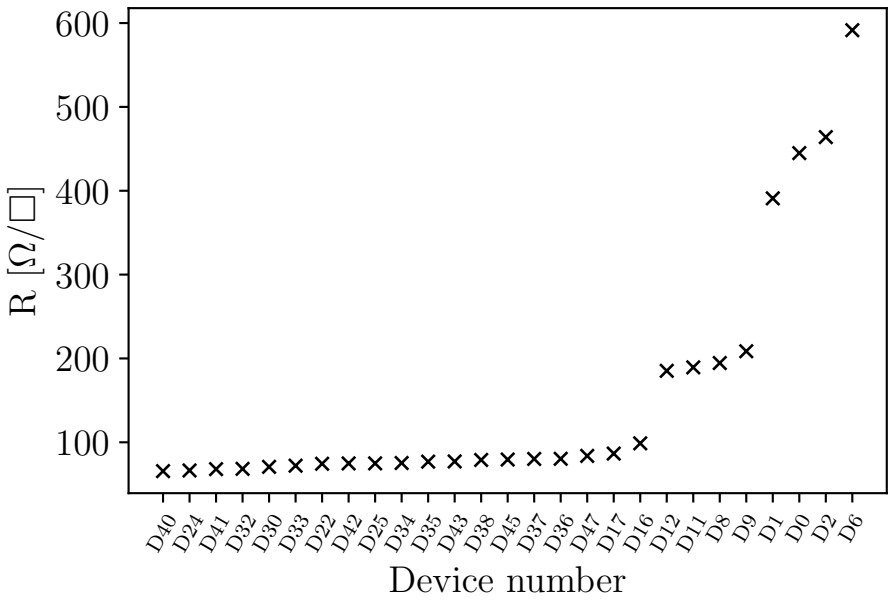

Figure 5.11: Measured palladium resistances at 4K, sorted by resistance

done exclusively, giving more trust in the nominal values of height. Also, profilometer measurements gave heights of 9-10nm for the film, matching the nominal combination of Titanium and Palladium. Using thus the height $h = 5$ nm, I get a thin film cryogenic resistivity of

$$\rho_{Pd}(4K) = 390\ \Omega\,\mathrm{nm} \tag{5.2}$$

The reported literature value for 30nm thin films was $\rho_{Pd,Lit}(2K) = 80\ \Omega\,\mathrm{nm}$, to which my found resistivity is a factor 4.9 larger.

Critical currents of NbN structures

The last reported results concern the NbN-chip. Regarding the SNSPDs first, I measured eleven devices, from which six had detectable and reproducible critical currents. Their critical currents are reported in figure 5.13, the values range from 2µA to 4µA. One exemplary IV-Curve of a SNSPD is given in figure **??**, it has a critical current of 4µA and a hysteresis current of 2µA. The critical current of the SNSPDs is much lower than expected from literature, where values of 10-20µA for the same geometries are reported.

Regarding the Lines, I measured 26 devices, from which 21 had detectable and reproducible critical currents. These are plotted against the line width in figure 5.16. It can be seen that the results are quite scattered, too scattered to insert any reasonable linear fit. The highest critical current relative to the width is found for a line with $I_c = 200$µA and $w = 2$µm. Compared to the estimation 10µA/60nm that I employed throughout this thesis, the highest determined ratio is still almost a factor two smaller than in the

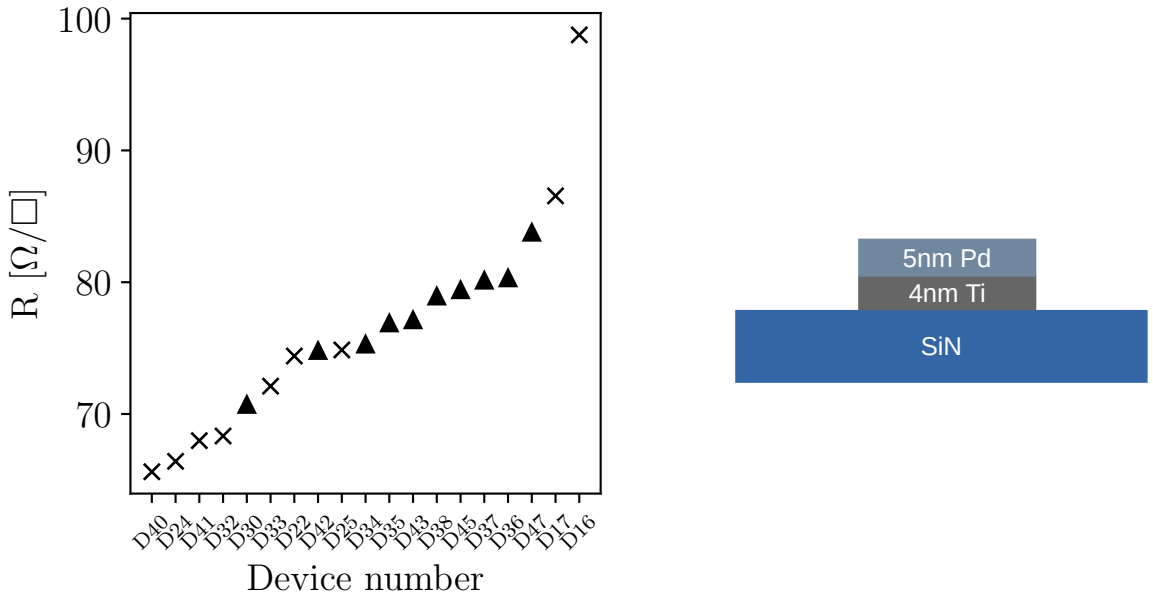

Figure 5.12: Resistance of palladium, including only data points for resistors at least 1µm wide and 10sq long. Data points marked with a triangles represent an even robust subset of resistors least 2µm wide and 50 squares long.

employed model, showing that my NbN-structures had significantly lower critical current than expected.

We also measured the cryogenic normal state resistances of the lines, those for which the value could be determined accurately are shown in figure 5.17. The values range from $R_sq = 250\ \Omega$ to $R_sq = 800\ \Omega$, a very wide range given that they all originated from the same thin film. It can be seen that for example amongst Since resistances should be less sensitive to small local imperfections as critical currents are, I don't have a satisfying explanation as to why they still differ to such a degree.

An example of one of the cleanest IV-Curves measured amongst the Lines is shown in figure 5.15, for a line with width 520nm. The critical current is at 33µA and the hysteresis current at 12µA.

Regarding the Meanders, I measured five, out of which only one showed a curve from which a critical current could be determined. It's IV-Curve is shown in figure 5.18, indicating a critical current at around 30µA. Given that the meander has a width of w=1.5µm, the in comparison small critical current would indicate that there is at least one significant local constriction along the meander due to fabrication imperfections.

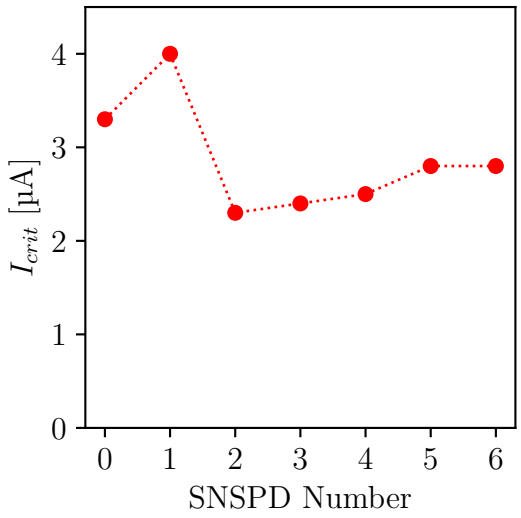

Figure 5.13: Critical current of six measured SNSPDs

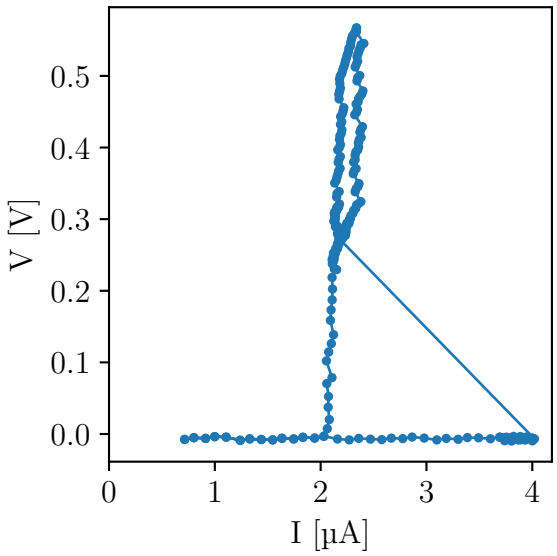

Figure 5.14: IV-Curve of the SNSPD with the highest critical current

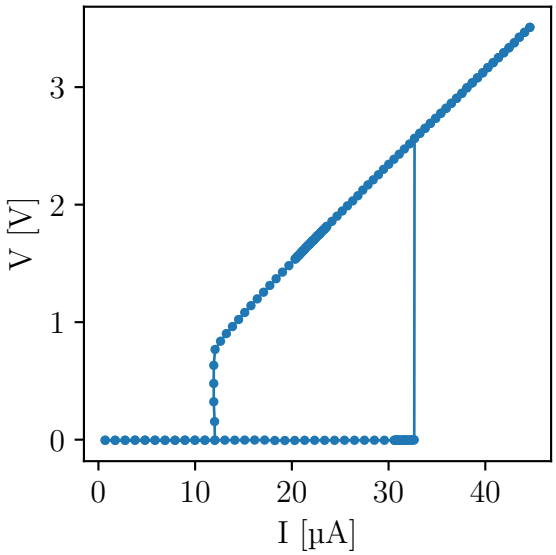

Figure 5.15: The cleanest measured IV-Curve for a line.

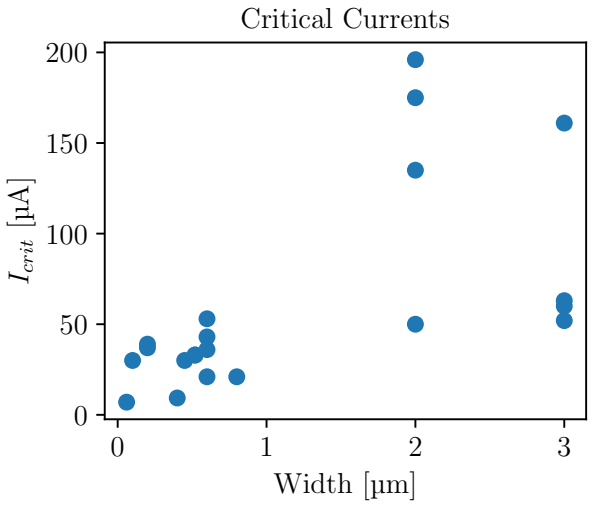

Figure 5.16: Measured critical currents for Lines with width different widths.

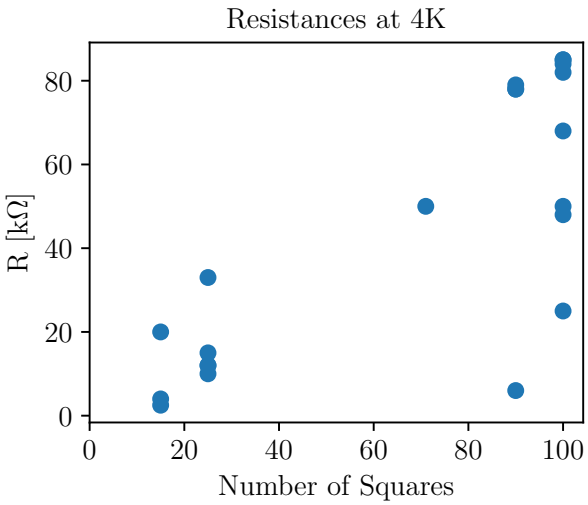

Figure 5.17: Measured normal state resistances at 4K for Lines of different lengths.

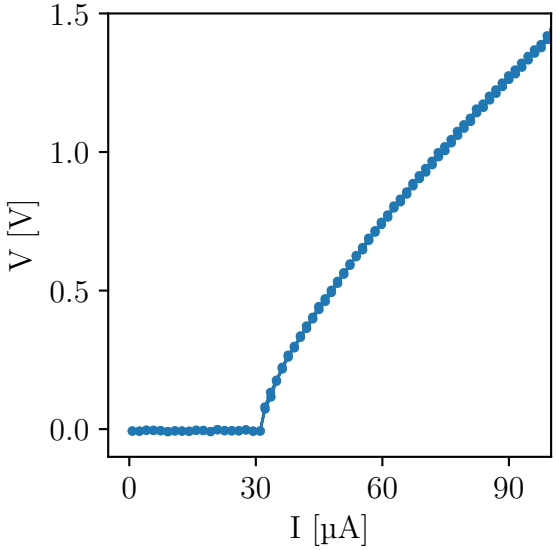

Figure 5.18: Measured IV-Curve for a Meander with w =1.5µm and N =10000 squares.

5.4 Conclusion of Chapter 5

The resistance measurements resulted in cryogenic resistivities of $\rho_{Au}(4K) = 64\ \Omega\,\mathrm{nm}$ for 15nm thin gold films and $\rho_{Pd}(4K) = 390\ \Omega\,\mathrm{nm}$ for 5nm thin Pd films. Compared to values in literature, the resistivity of gold was higher by a factor of 5, and the resistivity of Palladium was higher by a factor of 6. One possible explanation for that could account for much of the difference is that the resistivity itself is highly thickness-dependent for thin films [141], even though for bulk materials the resistivity allows to give thickness-independent values. This indicates that resistivities are not a good enough model for the resistances of thin films in the regime of few nm, and one would need to treat this topic with more care.

The NbN-measurements revealed that the critical currents on my chip were much lower than expected from literature. The SNSPDs had critical currents of 2-4µA, whereas reported values range between 10-20µA. The yield of the SNSPDs war 6 measurable devices out of 11.

For the Lines, the critical current showed even more scattering, and no sensible correlation with the width could be established by the given data. The yield was 21 measurable devices out of 26.

For the meanders, only one out of five devices showed an interpretable IV-Curve. It had a highly reduced critical current given the width, indicating that also along this meander there might be at least one significant local constriction.

Overall, the results for the resistors could be a useful first approximation for further designs, while the NbN-measurements were too scattered and the critical currents too low to be of any real use for future chips.

Chapter 6

Conclusion

In this thesis I investigated new approaches for optical readout of SNSPDs. I studied the interplay between interfacing circuits, SNSPDs and Electro-Optic-Modulators to identify properties of each individual element that could be used in combination to amplify the voltage provided by an SNSPD. I restricted myself to only use passive circuit components to keep the complexity and fabrication requirements low.

To this end, I found that optical readout allowed to exploit a to date rather unexplored property of SNSPDs: their states of high resistivity. I designed an interfacing circuit that exploited this seldom reached resistivity state of SNSPDs. This increased the generated output voltages by two orders of magnitude compared to previous circuits, which relied on electrical readout. This increase in voltage was large enough to reach the estimated required threshold for optical readout deduced from earlier published works, making the proposed interfacing-circuit a promising candidate also for experimental investigations.

The proposed circuit, which incorporates a NIR-sensitive SNSPD, has a reset time of 45ns, which would allow count rates up to ca. 20MHz. In comparison, the most closely related work by de Cea et al. was only sensitive for UV-photons and had a rest time of ca. 1µm, limiting the count rate to 1MHz.

The core ingredient to this circuit, the highly resistive states of SNSPDs, are widely known in literature. However, they were at times directly dismissed as "unlikely to be reached" and "implausible to occur", due to the assumption that every realistic circuit would need to have a connection to a 50 Ω transmission line. Via optical readout, however, no such transmission line is required, isolating the interfacing-circuit and the SNSPD from the contact to any low impedances. This allows the buildup of these elevated internal impedances and voltages as presented here.

I did extend the initial circuit design in two further ways, which did also increase the performance to some degrees, but only at the cost of highly increased fabrication requirements. In comparison to the provided output voltages, the two more complex circuits were not as efficient as the original first circuit which could be fabricated with much less demanding parts.

In one circuit I proposed the integration of a self regulated electro-thermal switch. Treating the thermal behaviour at cryogenic temperatures of such a switch evolved into it's own line of work and eventually into it's own chapter. I was able to show that it could be integrated successfully into an interfacing circuit for SNSPDs for optical readout. However, the resulting performance was only mediocre, limited severely by the high degree of coupling within the circuit. One main benefit regarding my treatment of this thermal switch might be thus in the work that allowed setting up the thermal simulations in the first place, which could help future members of the group starting into the topic of cryogenic thermal heat transport.

I did fabricate three integrated chips and charaterized them experimentally, giving new results in the resistances of cryogenic thin-films made from Gold and Palladium, as well as critical current values for superconducting NbN. However, the results for NbN were highly scattered and of rather low quality, limiting the useful results from the experimental section for future work to the gained resistance values.

Overall, one key interesting finding of my thesis might be that SNSPDs do show rich new dynamics within high-impedance environments, which might no longer be so "implausible", as optical readout could become a more and more realistic alternative to electronic readout.

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Appendix

As part of this thesis, two cryogenic amplifier boards have been designed, closely following [61]. For completeness we report here a few plots regarding them.

Two commercial SiGe-Transistors, BFP842 from Infineon and BFU725 from NXP, were compared, each soldered onto identical circuit boards. They were cooled from room-temperature to ca. 4K.

For transistor BFP842, the Gain increased continuously during the whole cooldown process, as shown in figure 6.2.

For transistor BFU725 instead, the Gain increased peaked at around T=78, and then decreased again, showing additionally some erratic behaviour at lower temperatures and lower frequencies, presented in figure 6.3.

Oscillations in the S21-curves were found out to not originate from the amplifiers, but from a badly matched VNA (ZVL 6). To counteract this bad matching, it was later learned that inserting 20dB attenuators to both the input and output ports of the VNA could suppress this mismatch and show the correct S21-curves.

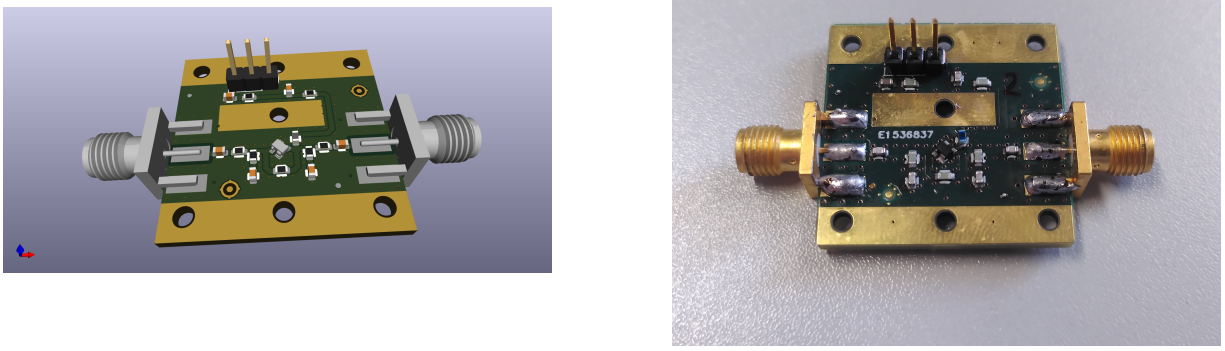

Figure 6.1: A Cryogenic Amplifier designed during this thesis. Design (left) and Photograph (right).

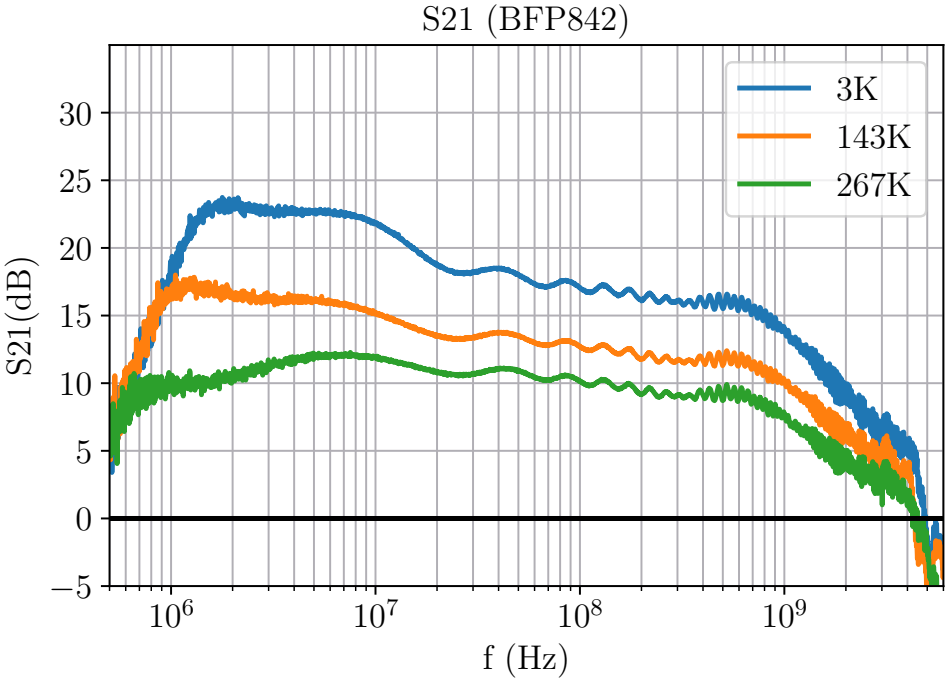

Figure 6.2: VNA-Measurement of the S21-parameter of Transistor BFP842 for three temperature regimes

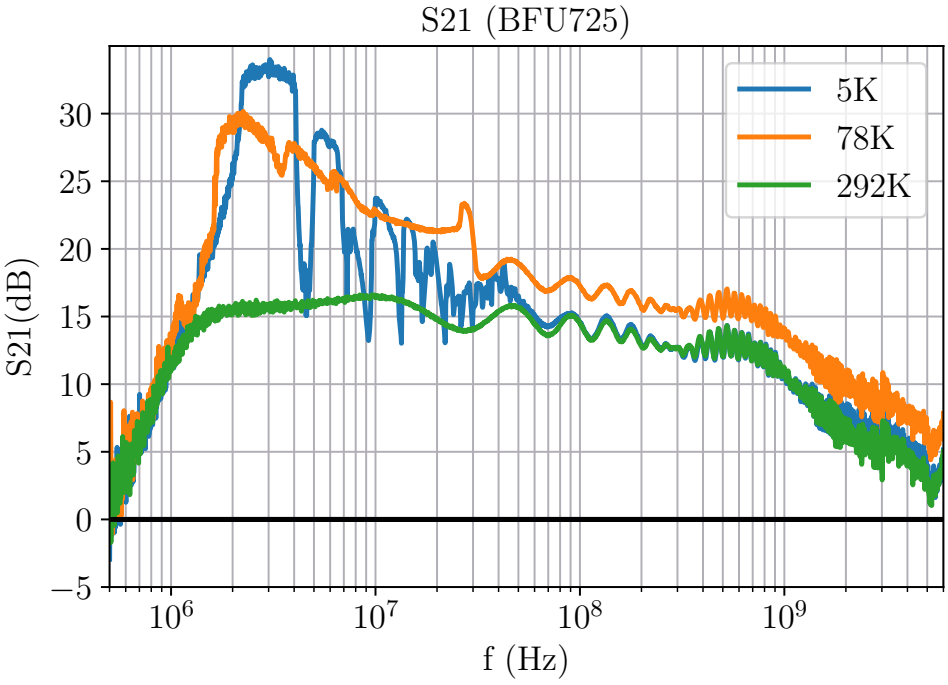

Figure 6.3: VNA-Measurement of the S21-parameter of Transistor BFP842 for three temperature regimes

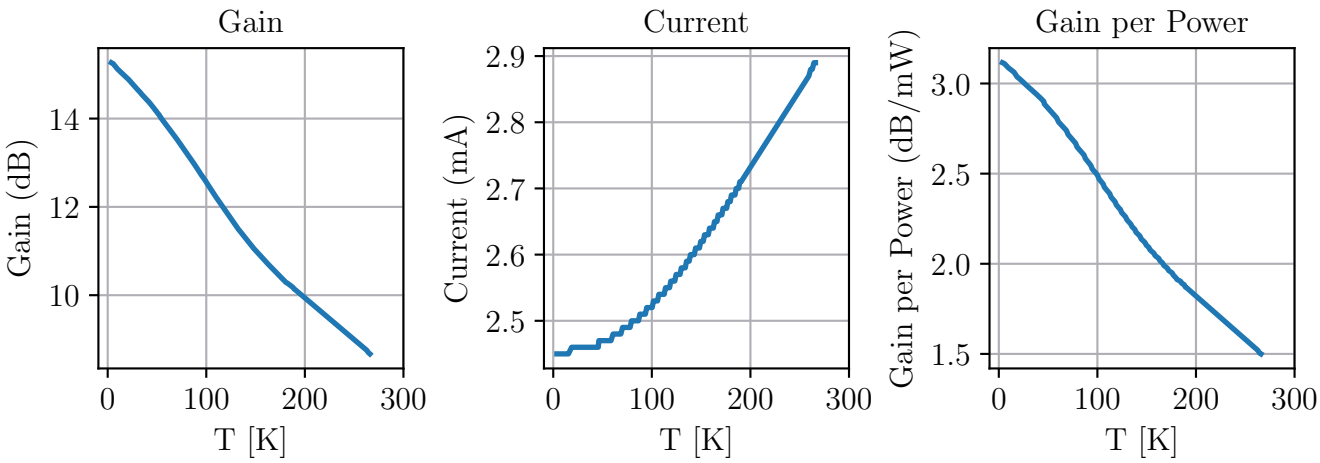

Figure 6.4: Dependence of the performance of the BFP842 transistor on temperature

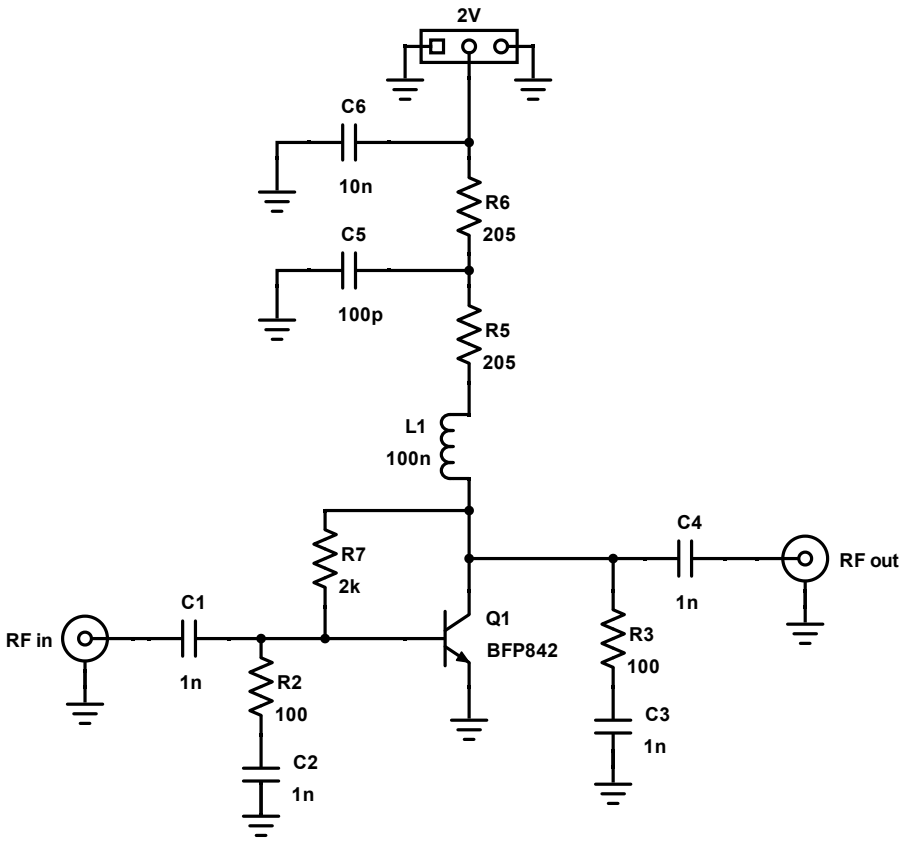

Figure 6.5: Circuit Schematic for the amplifier PCB

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